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RELIABILITY CHARACTERIZATION OF DIGITAL MICROCIRCUITS - INVESTIGATION OF AN IN-PROCESS OXIDE RELIABILITY SCREENING METHOD

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This report covers the work performed, using a sacrificial-metal-pattern technique, to demonstrate a 100% in-process screen for oxide defects in high-density CMOS microcircuits, and to evaluate the effectiveness and side effects of the added processing steps on yield and reliability. Using large-area polysilicon capacitors and 101-stage metal-1 delay-lines in GEM WAT keys as test vehicles, experiments with split lot reliability screening and life test, first with 240Å and again with 150Å gate oxide, have demonstrated practically complete elimination of the defective populations for test capacitors and about 50% reduction in circuit functionality failures for delay-line circuits. This is accomplished with little or no penalty in metal-polysilicon contact resistance, or in delay-line circuit yield. The technique is found to be promising and should be further investigated with more complex circuits with double-level metals.

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EVALUATION

The reliability of some microelectronics technology families is dominated or strongly influenced by insulator breakdown failure mechanisms. In past years, various aging and non-aging screen tests, and redundancy schemes have evolved to control oxide failures in product sold to customers. In recent years, increasing attention has focused on identifying root causes and eliminating them by making material, equipment, and process improvements.

Some customers require the best achievable reliability and the longest possible lifetime, since failures may directly cause loss of life and property, create unsafe situations, and inflate maintenance costs. Also, in some business sectors, system lifetimes are being extended far beyond original plans.

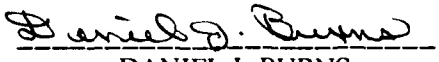
The challenge remains to not only deliver product which meets customer reliability requirements, but to maximize yield. Often this amounts to a conflict which must be resolved using models and test data to determine whether or not screening is needed, and if it is, how much. It is thought that today high voltage screens still play an important role in screening out potential early life insulator failures in both dynamic memories and random logic devices at several manufacturers.

If the distribution of oxide failures in time is zero until 30 years, then no screening is necessary for customers who require the best. On the other hand, if a wide or bimodal distribution of oxide lifetimes is known to exist or recur periodically in a product line, it is desirable to screen out the freaks to improve the early life failure rate of the remaining population. Contrary to some notions being popularized, screening sometimes can in fact improve the reliability of the remaining population of devices. This is so because reliability is defined as 1-(hazard rate), which is 1-(instantaneous probability of failure)/(1-cumulative failures). In some cases, screening can move the customer time zero reference to a point on the hazard rate curve where reliability is improved. Another important motivation for at least some screening is to generate failures or marginal parts which can be analyzed to determine root causes. This is a vital to continuous improvement.

Of course, screening will not necessarily make a good device better, although this may appear to occur. For example, a spot source of alkali ion contamination which might exist before burn-in may be more hazardous than a diffused blanket which might exist after a time at high temperature. Also, a MOS dynamic memory cell with a marginal low refresh time may exhibit longer refresh time after a high voltage screen which causes electron trapping which opposes tunneling at the cathode. If either of these situations were known to exist, the manufacturer would probably still search for process or test improvements to fix or screen such problem devices.

If the defects of concern are due to unassignable random causes, they will not be controllable by statistical process control. The root cause of the failures must be determined by analyzing failures generated by testing test structures or products. If the root causes cannot be identified or controlled to the level required, then screening is necessary. Aging oxide screens involve voltage, time, temperature stress to age above the freak population lifetime, but below the main population lifetime. Alternatively, a non-aging high voltage leakage current test may reveal the presence of defective oxides. Presently such inspection after fabrication is finished is impossible in many integrated circuits because achievable stress is limited by low junction breakdown voltages, and is confounded by the complexity of circuit function, and test pattern generation, which often interfere with application of even stress to all oxides. Although processes could be modified to support higher voltage, and built-in circuitry could be added to control screening, a simpler approach is to screen during fabrication.

In process gate oxide screening can be accomplished, yet has not been widely investigated in production environments to date. This effort was undertaken to investigate the cost and benefit of one approach to incorporating a controlled transistor gate oxide reliability screen into the fabrication process flow for CMOS integrated circuits. It uses a sacrificial metal layer to connect all poly gates in parallel to enable screening prior to drain connection. The results indicate that significant improvements in reliability result, with little or no effect on product reliability introduced by the added processing.



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PREFACE

This report covers the work performed, using a sacrificial-metal-pattern technique, to demonstrate a 100% in-process screen for oxide defects in high-density CMOS microcircuits, and to evaluate the effectiveness and side effects of the added processing steps on yield and reliability. Using large-area polysilicon capacitors and 101-stage metal-1 delay-lines in GEM WAT keys as test vehicles, experiments with split lot reliability screening and life test, first with 240Å and again with 150Å gate oxide, have demonstrated practically complete elimination of the defective populations for test capacitors and about 50% reduction in circuit functionality failures for delay-line circuits. This is accomplished with little or no penalty in metal-polysilicon contact resistance, or in delay-line circuit yield. The technique is found to be promising and should be further investigated with more complex circuits with double-level metals.

1. INTRODUCTION

1.1 General

The objective of this study was to demonstrate a 100% in-process screen for oxide defects in state-of-the-art digital microcircuits and to evaluate the effectiveness and side effects of the added processing steps on yield and reliability. This effort included the following tasks: literature survey, investigation of the sources of oxide defects, investigation of alternative approaches to accomplishing 100% oxide screening, and demonstration of an in-process screening technique.

1. *Literature Survey*
   Evaluate alternative approaches to oxide screening technique to improve circuit reliability through a literature search and original thinking.
2. *Sources of Oxide Defects*
   Investigate sources of oxide defects as a function of process steps, and evaluate impact of screening at various steps in the process flow.
3. *Alternate Approaches*
   Investigate alternative approaches to accomplishing a 100% screening of all oxide areas in MOS integrated circuits, with emphasis on transistor gate oxides, and evaluate alternatives in terms of the impact on design time, masks, layout rules and checks, fabrication steps, potential impact on yield, extra handling, and the resulting screening effectiveness.
4. *Demonstration of an In-Process Screening Technique*
   This involved choosing one of the alternatives for in-process oxide screening and performing a feasibility study to demonstrate application of the technique. This task included the following:
   a. Definition of oxide quality test to assess the need for an oxide reliability screen for a wafer, and for demonstration of the required parameters for in-process screening.
   b. Definition of specific implementation of the screening method and design of the additional process steps required to accomplish screening. This task involved identifying means for adding in-process screening to typical CMOS and CMOS-on-insulator technologies.

c. Test Vehicle Selection. This task involved development of a test/demo plan and selection of test vehicles to demonstrate the screening approach chosen. The test vehicles included a simple test structure and a logic circuit.

d. Split lot reliability screening and life test. This consisted of fabricating the test vehicles and applying the in-process screen to a portion of the sample population, and life testing the entire population to assess the effectiveness of the in-process screening. In this task, consideration was given to provide artificial introduction of defects, or special means to allow higher stress during life test as possible ways to ensure that the life test will be meaningful.

e. Failure Analysis. This consisted of analyzing test vehicle failures that occured during screening and the life tests in order to assess screening effectiveness.

1.2 Oxide Breakdown Strength Distribution

Silicon dioxide plays a vital role in modern integrated circuits. MOS ICs depend on the dielectric integrity of thin oxide layers for the high input impedance of MOS transistors and the charge storage capability of MOS transistors [1-40]. For reliable operation, it is important that the integrity of the gate oxide be maintained throughout the fabrication process. As device geometries are reduced, gate-oxide thicknesses are scaled as well. Oxide thicknesses from 100Å to 150Å are currently being investigated for the next generation of ICs. Due to the importance of compatibility with existing circuits, these thin oxide devices are usually operated at the standard 5 V power supply which imposes very high electric fields across these thin oxides. Use of high electric fields makes it critical that thin oxides be free of defects for the ICs to operate reliably in the field. Accordingly, there is considerable interest in techniques to screen devices having defective oxides prior to their incorporation into equipment for field use [42-56].

A typical plot [41] of the logarithm of the number of transistors with defective gate oxide regions on an untested and unscreened silicon wafer vs electric field applied to the gate oxide for a given unit of time (such as 1 ms) is shown in Fig.1. The peak at the left represents devices which are initially shorted or short with a few volts applied for a very brief time. Devices with this type of defect, if fully tested electrically, would typically not be present in the population of devices shipped to a customer. The

second peak represents infant mortality failures in unscreened product during life testing or product usage and that may be minimized, in general, by proper growth, annealing, gettering or processing. E5 is the voltage to which the gate oxide should be stressed, if possible, to weed out defective devices. With many high-density devices, the voltage stress is, however, limited to E4. The peak on the right represents devices having gate oxide failure due to intrinsic oxide breakdown or to inherent oxide breakdown in certain types of transistors.

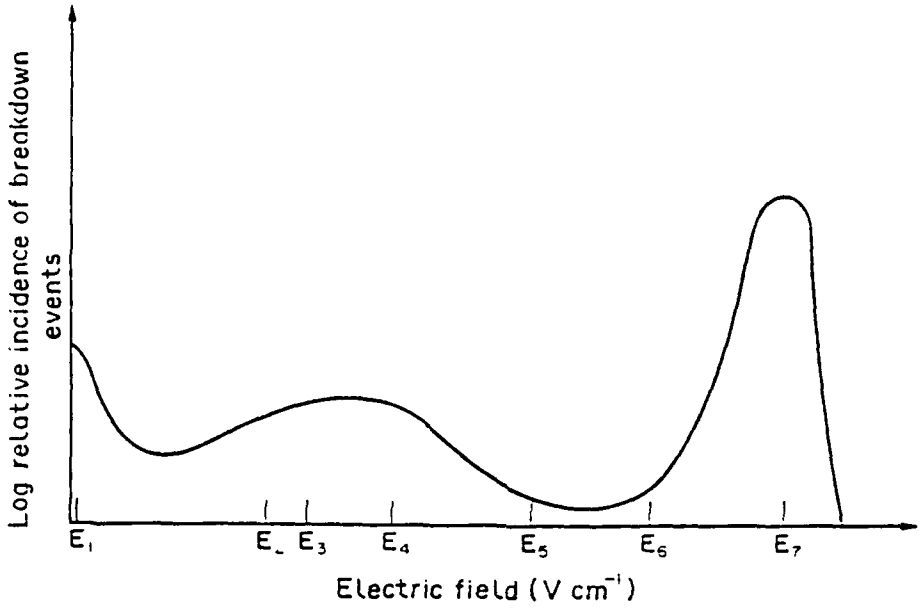


Figure 1. Plot of number of gate oxide defects in an integrated circuit vs electric field across the gate oxide.

When several types of active devices or several types of thin-oxide structures exist in an IC, several types of inherent breakdown may exist, and each type of device or structure may contain localized defects that are potential infant mortality defects. For example, ICs containing two or more levels of polysilicon, both the gate oxide and the oxides over polysilicon can contain defects that adversely affect reliability. Transistors (or capacitors) free of localized defects, but containing topology that results in high electric fields or oxide thinning at the topology features, may have an inherent gate oxide breakdown voltage that is substantially lower than the intrinsic breakdown of planar oxides on the same wafer. The ratio of the

inherent transistor (or capacitor) breakdown voltage to the intrinsic breakdown voltage of the planar oxide provides an indication of the merit of the process in terms of minimizing or overcoming topology effects. It is known that processing conditions can be changed to obtain significant increases in the dielectric breakdown voltage of devices with topology. These process changes can have a favorable impact on reliability, since they permit voltage stressing and/or burn-in at higher voltages.

In order to ensure high reliability or low failure rate of ICs in field use, the defect population shown in Fig. 1 must be eliminated. The most common method for screening oxides is burn-in. This typically involves operating a device at a higher-than-normal voltage level and/or at an elevated temperature for a prescribed period of time [59,60]. Extensive studies of dielectric breakdown of MOS device structures have shown trimodal distribution of breakdown voltages similar to that in Fig.1 [69-72]. These studies also show that the voltage acceleration factor for time-dependent dielectric breakdown is very high, whereas the temperature acceleration factor is relatively low [61]. The most commonly reported value for the temperature effect is an activation energy of 0.3 eV. Accordingly, the use of higher voltages is more effective than the use of higher temperatures in screening to eliminate devices having defective oxide sites which would be susceptible to time-dependent dielectric breakdown during field usage; hence the voltage-acceleration approach has been used in this study.

2. LITERATURE SURVEY

A literature search was conducted in January 1991. Included was an on-line computer search of titles and abstracts, using INSPEC, from 1984 to date, AND an ISI Science Citation search of articles which cited two selected references (McPherson et al., IRPS, 1985; Lee et al. IEEE Trans. ED, Dec. 1988). A total of 140 references were found in the INSPEC search, using "oxide breakdown" and "oxide reliability" as key words. Sixteen references were found in the ISI search. A listing of the computer search of titles is provided in Appendix A. These were supplemented by other references from our files. Earlier literature is broadly covered in the references cited in a number of the more recent articles that were obtained during the search. Selected publication copies were reviewed relative to the objectives of the contract.

Alternative approaches to in-process oxide screening range from application of a voltage stress immediately after gate oxide formation to application of a voltage stress at the last possible step in the wafer process sequence. Available published information continues to indicate that the oxide defects can be formed at a number of wafer process steps after gate oxidation, and thus application of the 100% voltage stress after high-temperature processing (after patterning of polysilicon and flow and reflow of PSG or BPSG) offers the best opportunity to screen defects that may have occurred in earlier process steps such as ion implantation or plasma etching. The best overall tradeoff for silicon-gate CMOS ICs is believed to be the use of a sacrificial metal pattern to simultaneously apply voltage to all the gates, relative to the underlying MOS transistors. A detailed discussion of alternative approaches, sources of oxide defects, and impact of alternate approaches are given in Sections 3 and 4.

In accordance with Section 4.1.8.4 of the Statement of Work, we chose the sacrificial metal pattern technique as the best approach to 100% in-process oxide reliability screening.

3. SOURCES OF OXIDE DEFECTS

The sources of oxide reliability failure defects can be categorized into (i) process-related oxide defects, and (ii) material-related oxide defects. These are listed in Table 1.

Table 1. Sources of oxide defects.

A. Process-related Oxide Defects:
- Non-uniform oxidation
- Mobile ion contamination during oxidation
- Pattern edge/corner
- Gate-oxide-related photolithography
- Residual nitride on Si surface
- Ion implantation
- Reactive ion etching
- Resist ashing
- Jet scrubbing
- Static electricity
- High-temperature

B. Material-related Oxide Defects:
- Oxygen micro-precipitates
- Metallic impurities (e.g., Cu, Ni, Na) in the oxide
- Contaminated crystal defects
- Imperfect Si surface polishing
- Non-smooth Si etching
- Flaws and scratches in silicon
- Si micro-powder left on the surface

3.1 Process-Related Oxide Defects

Process-related oxide defects [62-68] include defects introduced into the oxide either during the oxide growth process due to non-uniform oxidation because of stress in the Si/SiO_2 interface, or contamination of mobile ions, or radiation damage or charging damage during subsequent device processing operations such as ion implantation, plasma etching and resist ashing.

Non-uniform oxidation of silicon leads to localized oxide thinning which causes local electric field intensification across the oxide, leading to

degradation of long term oxide reliability. When the silicon surface prior to gate oxidation is neither planar nor smooth, such as at the edge of trenched silicon, oxide thickness uniformity depends on the oxidation [73,74]. Oxide thinning at patterned silicon edges and corners has been attributed to oxidation suppression due to stress increase in the oxide following a volume expansion at the Si/SiO_2 interface [75-78].

Another common cause of oxide thinning in CMOS and BiCMOS process is residual silicon nitride, Si_3N_4, on a silicon surface. The Si_3N_4 film is commonly used as a mask during LOCOS (local oxidation of silicon) oxidation [79]. E. Kooi et al [80] found that the gate oxide grown after the LOCOS process showed a thin ring around the periphery of the pattern. The model they proposed, which is largely accepted, states that during wet oxidation the Si_3N_4 masking layer is also oxidized, thereby forming some kind of ammonia species, which diffuses through the masking Si_3N_4 and pad SiO_2 and reacts with the silicon underneath, growing a thin nitride layer. This layer of Si_3N_4, if not completely removed, will retard oxidation in the area, leading to non-uniform oxidation. Ormond et al [81,82] relate low gate oxide breakdowns to area-related film defects where chemical attack of the silicon occurs through pinholes, and to the edge effect as described by Kooi et al [80]. A simple method to eliminate the "Kooi effect" is the addition of 2% HCl during the wet isolation oxidation [83] and/or to include a sacrificial oxidation prior to gate oxidation [84], thus improving the dielectric characteristics of the thin gate oxide.

Electrical charging of semiconductor wafer surfaces during ion implantation has been reported by numerous papers in recent years [85-88]. The problem is especially pronounced in high-current implanters used for advanced ICs with gate oxide thickness of 200Å or less. In these applications, the very high rate of charge deposition and induced charges on the surface of 4- to 8-inch-diameter wafers can cause serious damage to the wafers and the oxide layers in the devices or circuits, ranging from macroscopic poor implant dose uniformity [88] to microscopic deterioration of individual devices [87]. The macro-charging effect is caused by charging of the entire wafer surface, leading to changes in the ion-beam profile at the wafer plane and results in a non-uniform implant. The micro-charging effect is the result of localized microscopic trapped charges within or near the insulating oxide layers. These trapped charges can generate large local electric fields across thin dielectric layers and destroy the thin dielectric layers or degrade oxide reliability. High electric fields across thin oxide layers can also cause electron tunneling from the substrate or micro-discharges along defects, resulting in softened device characteristics and

long term reliability problems [87]. Wu et al [88] demonstrated that proper electron-flood-gun control using an in-situ capacitive-charging pickup sensor can eliminate wafer charging during ion implantation, thus resulting in improved reliability.

Charge buildup on conductors is also the primary cause of oxide damage during plasma etching [89-92, 94-100], resulting in gate oxide leakage or breakdown. Recent data [101-103] show that plasma non-uniformity across the wafer surface is mostly responsible for the oxide damage since it produces electron and ion currents that do not balance locally. Fang et al [105] used both direct plasma-probe measurements and circuit models for the plasma currents to calculate the current flow through MOS capacitors on a silicon wafer, and as able to match the observed damage with the calculated Fowler-Nordheim tunneling current through thin oxide layers. The relationship between Fowler-Nordheim tunneling current and oxide damage involves the injection of electrons that produce trapped holes near the gate/oxide interface, thus enhancing the electric field and the stress on the gate oxide and causing degradation in long-term oxide reliability even if early breakdown is not produced.

Plasma ashing of patterned photoresist can also damage oxides [104]. During ashing, gate oxides are more susceptible to charging damage since they typically start as isolated islands and the areas exposed to the plasma increase as the protective photoresist is etched. Use of wet stripping or ashing in a nonplasma ozone asher can avoid charging damage to the oxide during plasma ashing [93].

Charge buildup on patterned wafers can also occur during wafer processing steps such as jet scrubbing and spin drying. Measurements with static-charge meters have shown that during these processing steps, the patterned conductors on the wafer surface can be charged to several hundred volts. This amount of friction-induced charging can easily cause dielectric breakdown or degradation in thin gate oxides [88]. To eliminate this wafer charging, jet scrubbing and wafer spinning are often replaced by more gentle cleaning techniques such as rinsing in alcohol to dry wafers.

Oxide degradation after high-temperature post-oxidation anneal has been studied by many investigators [116-118]. Holland and Hu [106] found that for post-oxidation annealing temperatures higher than the oxide softening temperature (~950°C), the viscous shear flow or the creation of oxygen deficient sites in the SiO_2 causes a dramatic increase in hole trapping efficiency. This in turn decreases the oxide charge-to-breakdown (Q_{BD}). On the other hand, annealing at 800°C or less does not

affect Q_{BD}. They also reported that oxide Q_{BD} can be maximized by keeping the oxide oxidation temperature below 1000°C and the optimum post-oxidation annealing temperature is approximately 900°C. These results are consistent with the recent data reported by Mehta et al [107] on post-growth process-induced degradation in thin gate oxides. They found that the degradation of gate oxide quality in terms of Q_{BD} with post-oxidation high-temperature annealing occurs only when the annealing is performed in the presence of polysilicon layer over the gate oxide. Annealing before polysilicon deposition does not affect Q_{BD}, suggesting thereby that the Q_{BD} degradation is not merely caused by the viscous shear flow of SiO_2 but by virtue of its flow in the presence of the overlay polysilicon film defining the gate. It is the shear flow at the two interfaces, i.e. polysilicon/SiO2 and Si/SiO_2, that causes stress buildup in the oxide film, leading to the degradation in gate oxide quality.

3.2 Material-Related Oxide Defects

Some oxide defects are related to the quality of the starting silicon wafers, such as oxygen micro-precipitates [108-113], metallic impurities [114,115], and contaminated crystal defects. It has been reported that SiO_2 grown on float-zone (FZ) Si material has less defects than that of Czochralski (CZ) Si [119, 120]. In CZ Si substrates, the concentration of oxygen exceeds the solid solubility at the process temperature and are included as interstitial atoms. These interstitial oxygen atoms can lead to oxide defects after oxidation of the Si substrate. However, in SiO_2 films at room temperature, interstitial oxygen is rarely encountered alone but combined with foreign species such as Na, H, etc. impurity ions to form more complex defects. Yamabe et al [121] presented conclusive evidence that oxygen micro-precipitates in Si substrates become oxide defects when they are included during oxidation. Impurity atoms can enter the grown oxide for many reasons, and at many steps of the fabrication process steps previously discussed. They enter the SiO_2 during oxidation if they are already present in the Si substrate, such as doping atoms P, B, As and various other impurities. Or, they have been incorporated voluntarily or involuntarily, such as H_2O and chlorinated compounds, in the oxidizing ambient. They can also be incorporated during many of the post-oxidation processing steps. For instance, post-oxidation annealing in H_2 or $H_2 + N_2$ mixture let H_2 enter the oxide, wet-etching steps let in contamination of alkali ions, metallization steps, and post-metallization anneals let in metallic ion contaminants. Plasma-etching steps introduce all sorts of impurities. Ion implants of the silicon substrate through a gate oxide

introduce intrinsic defects through displacement damage as well as impurity atoms. Lithography with electron beam or x-rays generates electron-hole pairs in the SiO_2, causing bond rupture and displacement damage. Finally, sodium-ion contamination continues to be a potential problem in all IC processing steps in spite of all kinds of precautions [120].

A number of reports have been published on oxide defects originating from silicon substrates [124]. Itsumi et al [123] showed that the sacrificial oxidation procedure is effective in removing oxide defects. Yamabe et al [124] reported that the major origin of B-mode oxide defect are oxygen micro-precipitates and metallic contamination in the Si substrates, and that to increase the reliability of thin thermally grown SiO_2 films, high-temperature pre-oxidation annealing to get rid of oxygen precipitates near the silicon surface and/or phosphorus diffusion into the back side of wafers to getter metallic impurity atoms such as Cu, Ni, and Na are required to achieve device yield and reliability at an acceptable level.

Other material-related oxide defects may originate from a nonplanar silicon substrate surface which results from imperfect silicon surface mirror polishing [127-129], microroughness of the silicon surface due to too much NH_4OH in SC-1 cleaning solution [129], non-smooth silicon etching by chemical dry etching or reactive ion etching (RIE) [126], silicon micro-powder left on the substrate surface, or simply flaws and scratches on the silicon surface. In these cases, the thickness of the thermally grown SiO_2 will not be uniform and thus constitutes an oxide defect and leads to premature breakdown and degradation in long-term reliability.

4. ALTERNATE APPROACHES FOR OXIDE SCREENING

4.1 Limitations in Applying Voltage Screens to Completed MOS ICs

The merit of voltage screening of IC wafers or packaged IC circuits have been extensively documented in the literature [3, 130-134]. In order to perform voltage screening to a completed MOS IC, it is necessary to apply the stress voltage to all the gates of the transistors in the circuit. However, under the application of a normal test vector set, some gates in the circuit will receive far more stressing than others. In addition, application of a stress bias to a packaged high-density IC may be constrained by the input protective circuit, the avalanche breakdown voltage of the drain junctions, punch-through, latch-up, and/or inversion of the field oxide. Moreover, the process of applying sufficient stress to one gate in the circuit may cause another gate to be unacceptably aged and result in excessive yield loss [37]. As a result, voltage stressing is becoming less utilized in screening gate oxides in completed MOS ICs, especially in random logic devices, because it requires a set of test vectors that stress each gate equally. To avoid these limitations to circuit stressing and to permit sufficient stress to be applied to all gates for a time period long enough to eliminate circuit chips with defective oxides, the voltage stress on the gates can be applied only during chip fabrication.

4.2 In-Process Oxide Stressing

Two possible methods for in-process application of gate stresses are (i) use of a sacrificial metallization pattern (or preliminary polysilicon pattern) to connect in parallel all of the polysilicon gates, and (ii) use of an electron or ion beam to charge the oxide before polysilicon deposition, or to charge the polysilicon after polysilicon gate formation [135].

For the sacrificial-metal-pattern method, a voltage stress is applied to all of the polysilicon gates of a silicon-gate MOS IC during wafer processing. After patterning of the n^+ polysilicon and the flow and/or reflow of the passivation/planarization glass, a sacrificial metallization pattern would be applied to connect in parallel all of the polysilicon gates. In this procedure, wafers that have contact openings made using the normal contact-cut pattern are aluminum metallized, and the metal is delineated using patterns specifically designed to interconnect all of the polysilicon lines to a broad metal stripe in the bond pad area. Metal is left over areas of contact to single-crystal silicon regions such as source and drain diffusion areas, but these metal regions are not connected to the

metal pattern which interconnects all of the gates. Voltage stressing is performed on each chip by probing the broad metal stripe in the bond pad region of each chip. A single probe may be used to step across the broad metal stripe, hence, once on each die. Alternately, a "bed of nails" could make electrical contact to each broad metal stripe area in each die in one operation. When electrical contact has been established with a broad metal stripe in one die area and another electrical contact made to the backside of the wafer, a brief high voltage screen is applied across each die area and the resulting current measured. This forces the same voltage on each gate electrode in each die area. If any gate oxide in the die area is defective, the die area will draw an abnormally high current, or an abnormally low current as in the case of catastrophic breakdowns in the metallization due to electrical shorts, and be detected as a failure. The failed dies can be "inked" in the usual fashion so that they are not sent for packaging after dicing. The screening voltage and its duration of application should be carefully chosen so as not to unfavorably affect the remaining lifetime of the devices with good gate oxides. The voltage stressing sequence can apply one polarity, or apply both positive and negative voltage to the interconnected polysilicon gate regions, relative to the silicon substrate back contact. Following this screening operation, the patterned Al metal layer used for contacting the polysilicon gates is stripped and then re-metallized with Al, Al-Si, or other Al alloy, and processing continued in the usual fashion.

The preceding discussion applies to techniques for in-process voltage stressing of conventional silicon-gate MOS IC wafers, or wafers with other refractory-conductor gate materials. With minor modifications, in-process voltage stressing can, in most cases, also be applied to silicon-gate MOS devices with buried contacts, to Al-metal-gate MOS devices and to other types of device structures.

A non-metal-contact method uses an electron or ion beam to either charge the gate oxide directly or charge the polysilicon gates. The electron or ion beam may be scanned electrically and/or mechanically over the entire wafer or batch of wafers in order to simultaneously charge all the gates on a wafer. The required stress potential can be maintained for a specified time by capacitively monitoring the potential of the gate areas [88] and using a feedback loop to the beam source.

4.3 Advantages and Limitations of In-Process Screening

The advantages of in-process voltage screening are:

- Screening results in a higher probability of producing products with high reliability.
- With in-process screening, higher voltages can be applied than would be possible with completed wafers or with packaged devices.
- All gate-oxide areas are stressed for equal times.
- Early feedback data can provide information on the oxide failure distribution and/or process contamination problems.

The advantages and disadvantages of using a sacrificial metal mask or of using ion or electron beam for in-process oxide stressing are tabulated in Table 2. Use of ion or electron beam for in-process oxide stressing has the advantage of not requiring any additional photomask patterns, metallization, photolithography, or metal etch steps and, therefore, less process complexity and little or no adverse impact on product yield or reliability. It has several disadvantages. Since the voltage stress is applied early in the process, it is thus not able to screen devices with damage occurring in subsequent steps after polysilicon gate patterning. As discussed in Section 3.1, many process steps subsequent to polysilicon-gate patterning in a typical CMOS or BiCMOS IC fabrication have been shown to have the potential for degrading gate oxides. With ion or electron beams for in-process voltage stressing, it is difficult to control the voltage-stress polarity since the secondary-electron-emission ratio of the surface bombarded by an ion or electron beam depends on a large number of parameters some of which are very difficult to control. Finally, ion- or electron-beam techniques, unless accompanied by a very sophisticated means for detecting incidence of oxide breakdowns (such as detection of light emission during breakdowns) provide no information on oxide defect density.

In-process stressing by the use of a sacrificial metal pattern after flow and/or reflow of passivation glass has the advantage of the screen being applied late in the wafer fabrication sequence, after all of the ion implantation steps and high-temperature process steps (600°C to 1100°C) have been completed. Typical subsequent steps are at 450°C or lower which are less likely to adversely affect the gate oxide. Another advantage

of using a sacrificial metal pattern for gate oxide stressing is the ability to stress the gate oxide with both positive and negative voltage polarity on the polysilicon gate electrode for n- and p-type devices with respect to the source and drain and/or the substrate underneath the gate oxide. The method is thus applicable to CMOS, BiCMOS, and CMOS-on-insulator technologies, whereas the ion or electron beam technique obviously is not. Lastly, use of a sacrificial metal pattern for voltage stressing has a high screening efficiency since it causes catastrophic damage at defects which can be easily mapped to provide information on oxide integrity and product yield.

Table 2. Alternate approaches of in-process oxide stressing - advantages and disadvantages.

	Sacrificial Metal Pattern	Ion or electron beam
Mask	Special mask needed to connect in parallel all polygates and to S/D	Not needed
Voltage stress polarity	Both + and - for n and p type devices	Difficult to control
Point of application	Can be applied late in processing to screen defects incurred just before metallization	Applied early in the process
Oxide defect	Can provide early info on oxide integrity and product yield	Cannot provide such information
Screening efficiency	Cause catastrophic damage at defects	May not cause catastrophic damage to give positive screen
Process complexity	Additional steps may adversely impact yield reliability	Less process complexity

Disadvantages of in-process stressing by the use of a sacrificial metal pattern include the need for a specially designed mask to connect in parallel all of the polysilicon gates and all of the sources and drains in each die on a wafer. This leads to increased process complexity, increased processing cost, possible adverse impact on device yield, and the

possibility of gate oxide damage at process steps subsequent to the in-process voltage screening, including the removal of the sacrificial metallization and the re-deposition of a metal or metal-alloy. However, the sacrificial metal layer used in in-process screening of gate oxides sees only limited temperatures, such as photoresist hard bake. There is no contact-alloying step so that there are no problems with metal spiking at contacts, total removal of the sacrificial metal by wet-etching [136], or residues that will prevent the formation of high-reliability, low-resistance ohmic contacts in the final metallization.

5. DEMONSTRATION OF AN IN-PROCESS SCREENING TECHNIQUE

5.1 Definition of Oxide Quality Test

Time-dependent dielectric breakdown (TDDB) of gate oxides of MOS transistors and of other thin-oxide structures is a principal failure mechanism in MOS integrated circuits [9-10, 132-133, 137-145]. In TDDB tests, MOS capacitors are biased at a fixed voltage and a fixed temperature for long times, usually about 1000 h. Time-to-fail for each device is recorded by automated computer test equipment and the data is analyzed by plotting the cumulative percent failure as a function of the logarithm of time-to-fail. TDDB tests have been used for many years as a process development tool and as an oxide reliability monitor for the fabrication of MOS circuits. Until recently [146], it has been widely accepted that the times-to-fail in TDDB are lognormally distributed[132, 147]. Figure 2 shows a typical TDDB lognormal distribution which can be approximated by the following expression for the failure density function, $f_s(\ln t)$ [132]:

$$f_s(\ln t) = \frac{1}{\sigma\sqrt{2\pi}(t-t_o)} \exp\left\{-\frac{1}{2}\left[\frac{\ln(t-t_o)-\ln\mu}{\sigma}\right]^2\right\} \qquad t \geq t_o \qquad (1)$$

where σ,μ and t_o correspond to the variance, mean and initial failure time, respectively. The values of these parameters are a function of the dielectric quality.

The occurrences of TDDB can be accelerated both thermally and electrically. Thermal acceleration is modeled by the Arrhenius equation as:

$$A_T = \frac{t_s}{t_o} = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_s}-\frac{1}{T_o}\right)\right] \qquad (2)$$

where T_s is the stress temperature, T_o the device operating temperature, and E_a the activation energy. The most commonly reported value for E_a is 0.3 eV, which is relatively weak compared to the acceleration due to electric field.

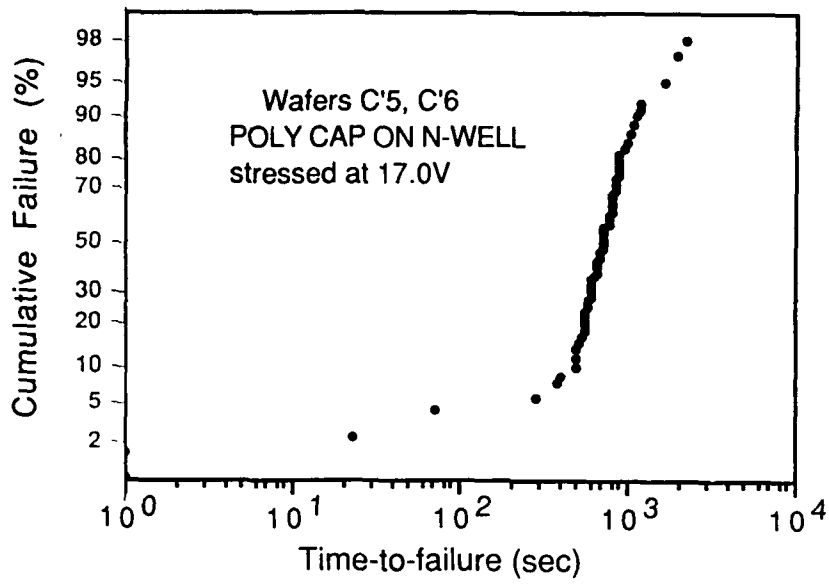


Figure 2. Typical TDDB lognormal distribution of failures of capacitors under constant voltage stress.

The electric field acceleration is modeled by a linear exponential dependence of electric field as

$$A_{EF} = \frac{t_s}{t_o} = \exp\left[-\gamma(E_s - E_o)\right] \tag{3}$$

where γ is an empirical curve-fitting parameter.

Thermal acceleration, A_T, and electric field acceleration, A_{EF}, are assumed to be independent, and therefore can be combined to give TDDB failures at device operation conditions from accelerated data:

$$f_s(\ln t) = \frac{1}{\sigma\sqrt{2\pi}(t-t_o)} \exp\left\{-\frac{1}{2\sigma^2}\left[\ln\left(\frac{t-t_o}{A_T A_{EF}}\right) - \ln\left(\frac{\mu}{A_T A_{EF}}\right)\right]^2\right\} \qquad t \geq t_o \tag{4}$$

This expression can be used to design a reliability screen (temperature and voltage) for a given device which will give the desired failure rate [132].

However, in recent years, several observations have been reported that affect the validity of extrapolation of product lifetime from accelerated TDDB measurements, using the above expression. First, the activation energy has been reported to vary as a function of the electric

field [148-150]. Second, the standard deviation of the lognormal failure distribution has been found to vary with both electric field and temperature, leading to an ambiguous acceleration factor determination [148-149]. Hu et al [146,151] proposed a reciprocal model in which the electric field acceleration factor is inverse-exponentially dependent on electric field, instead of linear-exponentially dependent, namely:

$$A_{EF} = \frac{t_s}{t_o} = \exp\left[-\gamma\left(\frac{1}{E_s} - \frac{1}{E_o}\right)\right] \tag{5}$$

It is shown that the reciprocal model has a quantitative physical basis, that is, oxide breakdown is due to Fowler-Nordheim tunneling and charge trapping at localized spots. The trapped hole density is modeled as [152]

$$Q_{ot}^{+} \propto J(E_{ox})\alpha(E_{ox})t,$$

$$\propto t\, e^{-(B+H)/E} \tag{6}$$

where Q_{ot}^{+} is the density of trapped hole charge, $J \propto \exp(-B/E_{ox})$ is the Fowler-Nordheim (F-N) current density and $\alpha \propto \exp(-H/E_{ox})$ is the hole generation coefficient [153]. At fields $\geq$ 6 MV/cm, the reciprocal field model of Hu et al have been shown to yield better agreement with experimental data in the literature [154]. However, at electric fields nearer to device operating conditions testing, extensive testing by Boyko and Gerlach [155] at fields $\leq$ 5 MV/cm in an attempt to determine electric field functionality has proven inconclusive. Neither a linear nor a reciprocal model accounts for their data of approximately 14,000 test capacitors over the entire range of temperature (60°C to 150°C) and electric fields (3 MV/cm to 8 MV/cm). Thus, we conclude that presently, the reciprocal field model is preferred over the linear field model for the following reasons:

- The reciprocal field model agrees better with experimental data at electric fields $\geq$ 6 MV/cm.
- The reciprocal field model has a quantitative physical basis, namely Fowler-Nordheim tunneling and localized charge.
- The reciprocal field model does not assume a lognormal distribution for TDDB. A lognormal distribution for a population with a defective sub-group is mathematically difficult to justify.

5.2 Voltage-Ramp-Oxide-Breakdown (VROB) Test

5.2.1 Oxide breakdown model

As mentioned in the previous section, according to the reciprocal field model the logarithm of the time-to-breakdown t_{BD} can be written as

$$t_{BD} = \tau_0 \exp\left[\frac{G}{E_{ox}}\right] = \tau_0 \exp\left[\frac{GX_{eff}}{V_{ox}}\right] \tag{7}$$

where V_{ox} is the voltage across the oxide, X_{eff} is the effective oxide thickness at the weakest spot in the oxide, and G = 350 MV/cm and τ_o = 1.0 x 10^{-11} s [156]. The concept of effective oxide thinning is used to model not only physical thin spots in the oxide film but also asperities at the interface and localized areas having a modified chemical composition which may increase the charge trapping rate or reduce the barrier height at the Si/SiO_2 interface.

By expressing $\tau_o(T)$ in Arrhenius form with activation energy E_b and expanding G(T) in a Taylor series in 1/T, we have

$$\tau_0(T) = \tau_0 \exp\left[-\frac{E_b}{k}\left(\frac{1}{T} - \frac{1}{300}\right)\right]$$

and

$$G(T) = G\left[1 + \frac{\delta}{k}\left(\frac{1}{T} - \frac{1}{300}\right)\right] \tag{8}$$

where δ and E_b have been experimentally determined to be 0.0167 and 0.28 eV, respectively [157].

Applying this model to situations with time-dependent voltage and temperature (e.g. ramp voltage testing and burn-in, etc), the incremental oxide damage $d\Delta$ incurred per unit time is assumed to have a damage rate dependent only on the instantaneous damage level and is independent of previous stress history, i.e.

$$\frac{d\Delta}{dt} = f(\Delta)g(V,T,X_{eff}) \tag{9}$$

where the functional form of f and g are to be determined. Integration gives

$$\int_0^{\Delta_{BD}} \frac{d\Delta}{f(\Delta)} = \int_0^{t_{BD}} g(V,T,X_{eff})dt = C \tag{10}$$

where Δ_{BD} is the damage threshold level for destructive breakdown. The constant C can be found by considering the constant voltage and temperature case:

$$C = g(V_{ox}, T, X_{eff})t_{BD} \tag{11}$$

Comparing Eq. (11) and Eq. (7), we have

$$g(V_{OX},T,X_{eff}) = \frac{C}{\tau_0(T)}\exp\left(\frac{-G(T)X_{eff}}{V_{ox}}\right) \tag{12}$$

Substituting Eq.(12) into Eq. (10), the breakdown condition for time-dependent voltage V = V(t) and temperature T = T(t) is obtained:

$$1 = \int_0^{t_{BD}} \frac{1}{\tau_0(T)}\exp\left(\frac{-G(T)X_{eff}}{V}\right)dt \tag{13}$$

Applying this to the case of ramp voltage test, V(t)=Rt and T(t)=T_t, where R is the ramp rate (in V/s), we have

$$\begin{aligned} 1 &= \int_0^{t_{BD}} \frac{1}{\tau_0(T)}\exp\left(\frac{-G(T_t)X_{eff}}{Rt}\right)dt \\ &\cong \frac{V_{BD}^{\,2}}{RG(T_t)\tau_0(T_t)X_{eff}}\exp\left(\frac{-G(T_t)X_{eff}}{V_{BD}}\right) \end{aligned} \tag{14}$$

where V_{BD}= Rt_{BD} [146]. In general, Eq. (14) has to be solved numerically to determine the X_{eff} corresponding to a measured V_{BD}. However, since the X_{eff} dependence of the exponential term dominates over the X_{eff} dependence of the pre-exponential coefficient, it is possible to obtain an accurate closed form solution for X_{eff} by setting X_{eff} in the pre-exponential term to 80 Å. This gives

$$X_{eff} \cong \frac{V_{BD}}{G(T_t)}\ln\left(\frac{V_{BD}^{\,2}}{RG(T_t)\tau_0(T_t)80\text{Å}}\right) \tag{15}$$

Substituting Eq. (15) into Eq.(7) gives the relation between V_{BD} of a ramp voltage test at temperature T_t and t_{BD} of a constant voltage V_{ox} test at T_t:

$$t_{BD} \cong \tau_0(T_t)\left[\frac{V_{BD}^2}{RG(T_t)\tau_0(T_t)80\text{Å}}\right]^{[V_{BD}/V_{ox}]} \qquad (16)$$

Since the ramp voltage test is much shorter than the constant voltage TDDB test, this is a very desirable relationship defining the ramp voltage test to characterize oxide quality and to project device reliability related to oxide quality. Wolters et al [158-162] also arrives at a similar conclusion, that there is no essential difference between time-dependent and ramp voltage oxide breakdowns. Both are consequences of the injection of charge to a critical value, Q_{BD}, through the oxide layer.

If a constant voltage screen is applied to the oxide before the voltage ramp test, the breakdown condition is the sum of the damage incurred during the screen, Δ_S and that incurred during the ramp test, Δ_t,

$$1 = \Delta_s + \Delta_t$$
$$\cong \frac{t_s}{\tau_0(T_s)}\exp\left(\frac{-G(T_s)X_{eff}}{V_s}\right) + \frac{V_{BD}^2}{RG(T_t)\tau_0(T_t)X_{eff}}\exp\left(\frac{-G(T_t)X_{eff}}{V_{BD}}\right) \qquad (17)$$

where the oxide is stressed at V_S *volts and* T_S *Kelvins for* t_S *seconds* and has a subsequent ramp test at T_t. This expression can be used to predict the ramp voltage breakdown after the in-process oxide screening.

5.2.2 Determination of voltage screen parameters

In order to determine an in-process screening voltage for any type of IC, it is necessary to know the typical distribution of oxide defects vs breakdown voltage, and also to know the inherent dielectric strength of the MOS transistors used in the IC. This information can be obtained most conveniently from voltage-ramp-oxide-breakdown (VROB) tests. Alternatively, the TDDB distribution can be used. According to the reciprocal field model of Hu et al, VROB and TDDB are equivalent and are related by Eq. (16). Since VROB tests are rather easy and quick while TDDB tests are time-consuming and expensive, VROB tests will be used to monitor gate oxide quality routinely and TDDB tests will be performed only on selected samples to verify correlation with VROB tests.

To determine the optimum screening procedure, the gate electrodes on a series of test devices are subjected to a ramp voltage at 1 V/s until oxide breakdown occurs. The cumulative percent failure is then plotted as

a function of the ramp oxide breakdown voltage V_{BD}. An example of the VROB distribution on a 500-transistor MOS array from a developmental process with t_{ox}=350Å is shown in Fig. 3 [41]. The VROB distribution measured at 55°C shows a break at the 20% failure level, indicating two failure mechanisms. The 20% of failure that occurs at the lower voltages are due to oxide defects, and the remaining 80% are due to inherent oxide breakdown. Obviously, the 20% defective population can be eliminated by a screening process in which the devices are subjected to a ramp voltage at 1 V/s at 55°C until the voltage reaches 25.5 V, at which point the applied voltage is turned off. Alternately, a constant voltage at 25.5V can be applied to the gate at a different temperature, T_S, for a time, t_S, which can be determined from

$$\frac{t_s}{\tau_0(T_s)}\exp\left(\frac{-G(T_s)X_{eff}}{V_s}\right)=\frac{V_S^2}{RG(T_t)\tau_0(T_t)X_{eff}}\exp\left(\frac{-G(T_t)X_{eff}}{V_S}\right) \qquad (18)$$

For a constant voltage screen performed at the same temperature as the VROB tests, $T_S = T_t$, we have

$$t_s=\frac{V_S^2}{RG(T_t)X_{eff}} \qquad (19)$$

where X_{eff} is given by Eq.(15) with $V_{BD}=V_S$.

Another criterian in the determination of an optimum screen voltage is that the voltage screen should not cause significant (>10%) wearout of the oxide in the rest of the good devices, i.e.:

$$\Delta_S=\frac{t_s}{\tau_0(T_s)}\exp\left(\frac{-G(T_s)<X_{eff}>}{V_s}\right)\le 0.1 \qquad (20)$$

where $<X_{eff}>$ is given by Eq. (15) with $V_{BD} = <V_{BD}>$, the average ramp oxide breakdown voltage for the intrinsic part of the VROB distribution. In the example given in Fig. 3a, $<V_{BD}>$ =28.0V, R = 9.4 V/s, $<X_{eff}>$ =197Å, V_S = 25.5 V, Δ_S = 0.086, indicating that the voltage screening process we have chosen does not significantly affect the wearout of the oxide in the good devices.

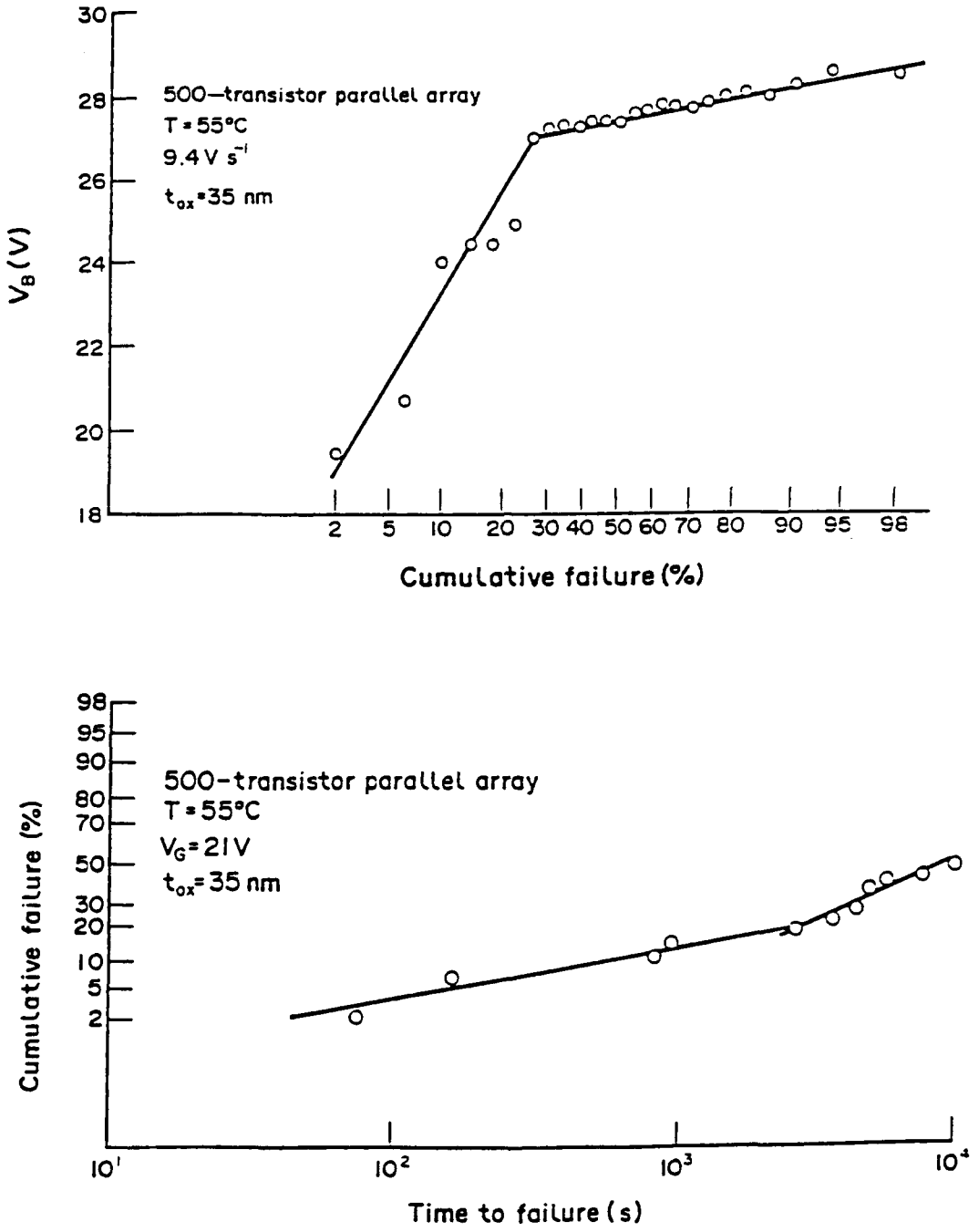


Figure 3. a) Voltage Ramp Oxide Breakdown distribution showing defect and inherent failure modes. b) Lognormal plot of time-dependent dielectric breakdown distribution showing defect and inherent failure modes.

5.2.3 In-process voltage screening for CMOS and CMOS-on-insulator technologies

In this section, we define the specific implementation of the screening method and design the additional process steps required to accomplish in-process screening to typical CMOS and CMOS-on-insulator technologies.

We begin by examining the structure of a typical bulk CMOS circuit, shown schematically in Fig. 4. The starting material is a lightly doped n^- epitaxial layer over a heavily doped n^+ substrate. The use of epitaxial wafers produces CMOS circuits that are less prone to latchup [163] when combined with proper circuit layout techniques. The p-tub and n-tub regions are formed by ion implantation and driven-in by diffusion to achieve carefully controlled surface dopant concentrations. This "twin-tub" CMOS approach allows the doping profiles in each tub region to be tailored independently. The NMOS and PMOS transistors are then fabricated in the p-tubs and n-tubs, respectively, and a tub may contain tens of thousands of transistors of a given type within it.

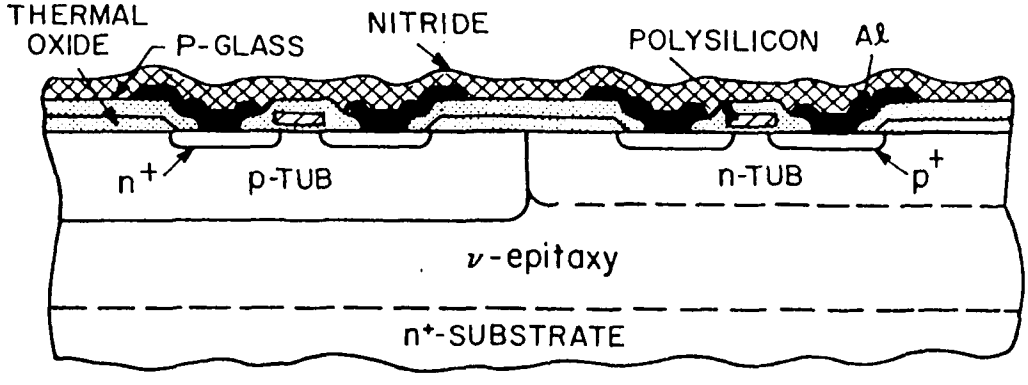


Figure 4. Schematic diagram of a typical bulk CMOS with twin tubs.

In order to stress the gate oxides effectively in both the NMOS and the PMOS transistors, the voltage applied must appear across the thin gate oxide underneath the entire gate and not across a depletion region underneath the gate oxide. Thus, for capacitors built on p-type silicon, the top electrode should be biased negatively with respect to the p-type substrate in order to properly stress the oxide layer. Figure 5 shows the I-V characteristics of a capacitor with 240Å oxide layer fabricated on p-type silicon substrate. With the n^+-doped polysilicon electrode biased

negatively with respect to the p-type substrate, the silicon surface underneath the oxide layer is accumulated, the leakage current through the oxide layer increases monotonically with the absolute value of the bias voltage across the oxide before oxide breakdown occurs at -28 V. However, with the polysilicon electrode biased positively with respect to p-type silicon substrate, the leakage current across the oxide layer levels off at ~+24 V and the oxide does not indicate any sign of breakdown even at 40 V. This is due to the formation of a depletion layer in the silicon surface underneath the oxide layer so that the applied voltage drops across the oxide layer and the depletion layer and results in a lower electric field across the oxide than it would be otherw

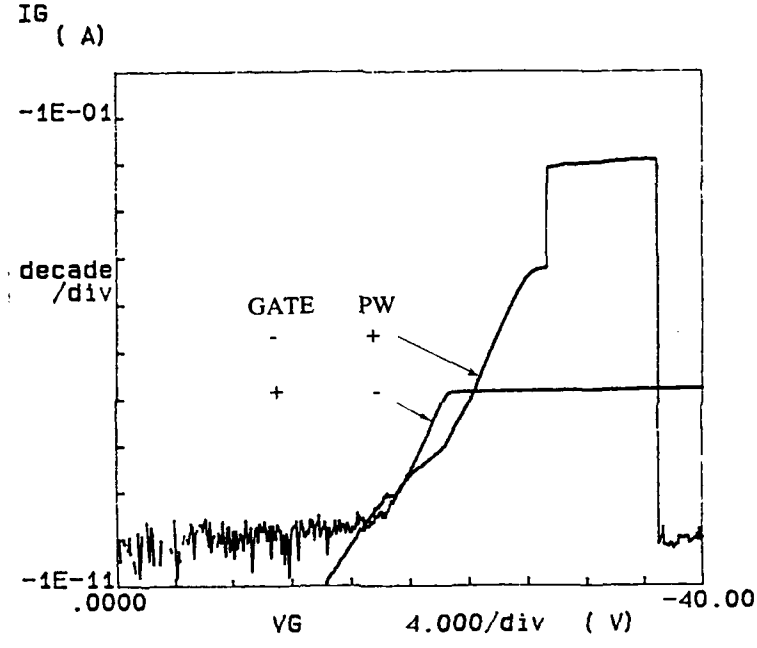


Figure 5. The I-V characteristics of a capacitor with 240Å oxide layer fabricated on p-type silicon substrate.

The situation, however, is somewhat changed in the case of an NMOS transistor in a p-tub in a typical CMOS circuit. An experiment was performed to investigate the feasibility of voltage stressing the gate oxide of NMOS transistor by biasing the gate positively with respect to the n^+ substrate on the back side of the wafer and the I-V characteristics are shown in Fig. 6. The leakage current as a function of the biasing voltage exhibits unpredictable features because the pn-junction at the edge of the

p-tub is reverse-biased and the potential of the silicon surface underneath the NMOS transistor gate is floating. Attempts to raise the pn-junction leakage current at the edge of the p-tub by raising the substrate temperature to 150°C only slightly alleviate the problem and do not eliminate it. Secondly, biasing the gate of an NMOS transistor with respect to the n+ substrate or the p-well alone does not adequately stress the gate oxide at the perimeter of the gate electrode which usually overlaps the source/drain regions. If contact can be made to the p-well substrate and electrically tied to both the source and the drain of the transistor, then the gate oxide can be adequately stressed by biasing the gate electrode with respect to the source/drain and the p-well substrate in a manner similar to the case of a capacitor already discussed. This is depicted in Fig. 7. If, however, contact to the well substrate is not available or easily accessible, the gate oxide of an NMOS transistor can still be adequately stressed when the gate electrode is biased *positively* with respect to the source and/or drain. When the gate electrode is biased above the threshold voltage of the NMOS transistor (typically 1 to 2 V), the channel regions of the transistor becomes conductive and the entire surface region underneath the gate oxide reached the same potential as the source or drain. Similarly, for a PMOS transistor, the gate electrode should be biased negatively with respect to the source and/or drain to stress the gate oxide. Reversing the polarities on the gate can lead to higher breakdown voltages since the gate oxide, in this case, is stressed only properly in the overlapped regions above the source and/or drain regions and improperly in the channel region. Thus, for both CMOS on bulk silicon and for CMOS-on-insulator, the recommended in-process screening method involves making parallel top surface connections to all of the gates and making a top surface contact to the source/drain, and stressing the gates both negatively and positively. This makes it simple to design a mask for sacrificial metal patterns in both bulk CMOS and CMOS-on-insulator technologies since sources and drains of transistors are typically connected together to V_{DD} or V_{SS} and a sacrificial metal pattern to connect together all transistor gates can be implemented with little or no penalty for modified contact and via layout.

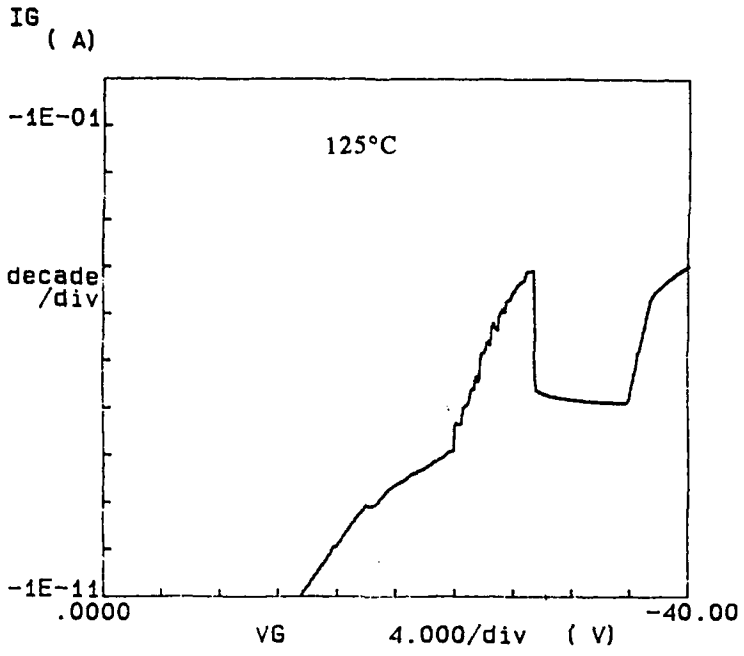


Figure 6. The I-V characteristics of a NMOS transistor in a CMOS circuit when the gate is biased positively with respect to the n+ substrate.

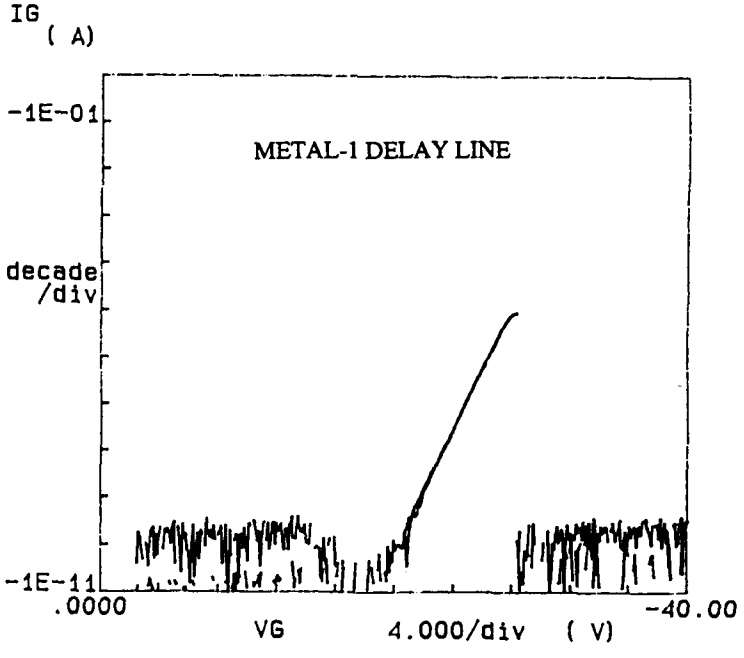


Figure 7. The I-V characteristics of a NMOS transistor in a CMOS circuit when the gate is biased positively with respect to the V_{ss}, and with respect to V_{ss} tied to p-well contact.

5.3 Test Vehicle Selection

An ideal test vehicle to assess the merit of in-process oxide screening is one designed for the state-of-the-art bulk CMOS technology, which contains both appropriate test patterns and a suitable logic device on the same wafer. One of the microcircuits currently being fabricated at Sarnoff's IC Center is based on a 1.5-μm BiCMOS technology with double-level metallization, and is used for the GEM (Generalized Emulation of Microcircuits) program [164]. The Wafer Acceptance Test keys contain a Metal-1 Delay Line circuit and large-area capacitors of thin gate oxides over p-type (p-well) and over n-type (n-well) regions of bulk silicon.

The Metal-1 Delay Line can be fabricated and tested using only one level of metallization. The delay line consists of 101 stages connected in series. Each of the 101 stages consists of a simple CMOS inverter having one n-channel and one p-channel transistor. The delay-line has no input protection circuits and its layout is shown in Fig. 8. The delay-line circuit is a simple logic circuit that is used in the present experiment to demonstrate the effect of oxide screening and extra processing steps on the yield of the circuit at the end of oxide screening and circuit fabrication. A sacrificial metal mask is fabricated to connect all of the gates of the delay line together for the purpose of voltage stressing the gate oxide after the delineation of the doped polysilicon gates but before the final metallization. The layout of the sacrificial metal mask is shown in Fig. 9. After gate oxide screening, the sacrificial metallization is stripped and the fabrication of the delay line finished with the proper metallization.

Large-area polysilicon capacitors over p-wells and similar capacitors over n-wells are used as test vehicles for oxide screening and subsequent reliability testing, and are shown in the photomicrograph of the GEM WAT keys in Fig. 10, together with the 101-stage Metal-1 Delay Line circuit. These capacitors measure 400 μm x 500 μm and consist of $POCl_3$-doped polysilicon over thin gate oxide. The thickness of the thin gate oxide is nominally 240 Å. The sacrificial metallization allows the voltage stressing on the thin oxide layers in these test capacitors prior to the final metallization.

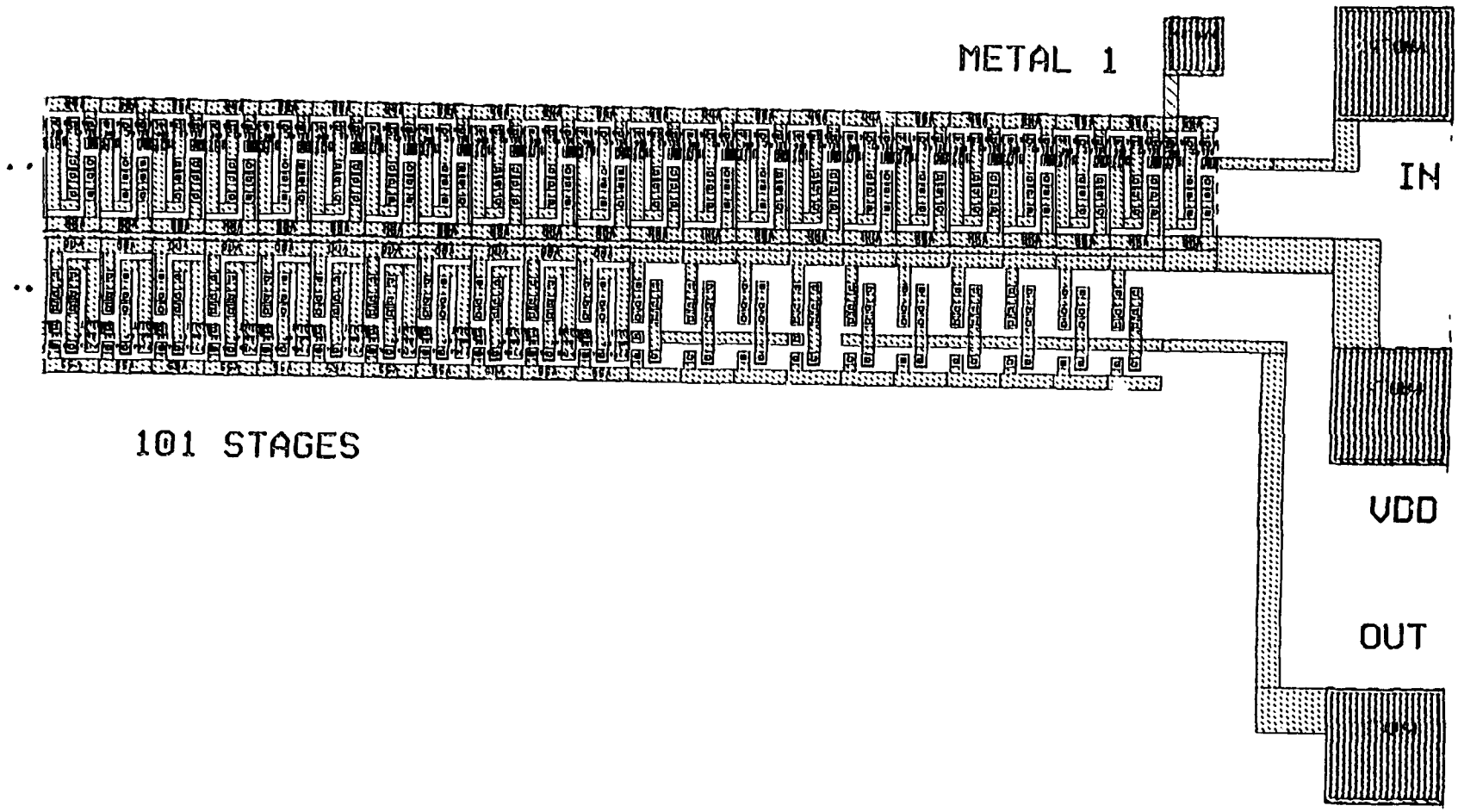


Figure 8. Layout drawing (with portions omitted) of the Metal-1 Delay Line circuit in GEM.

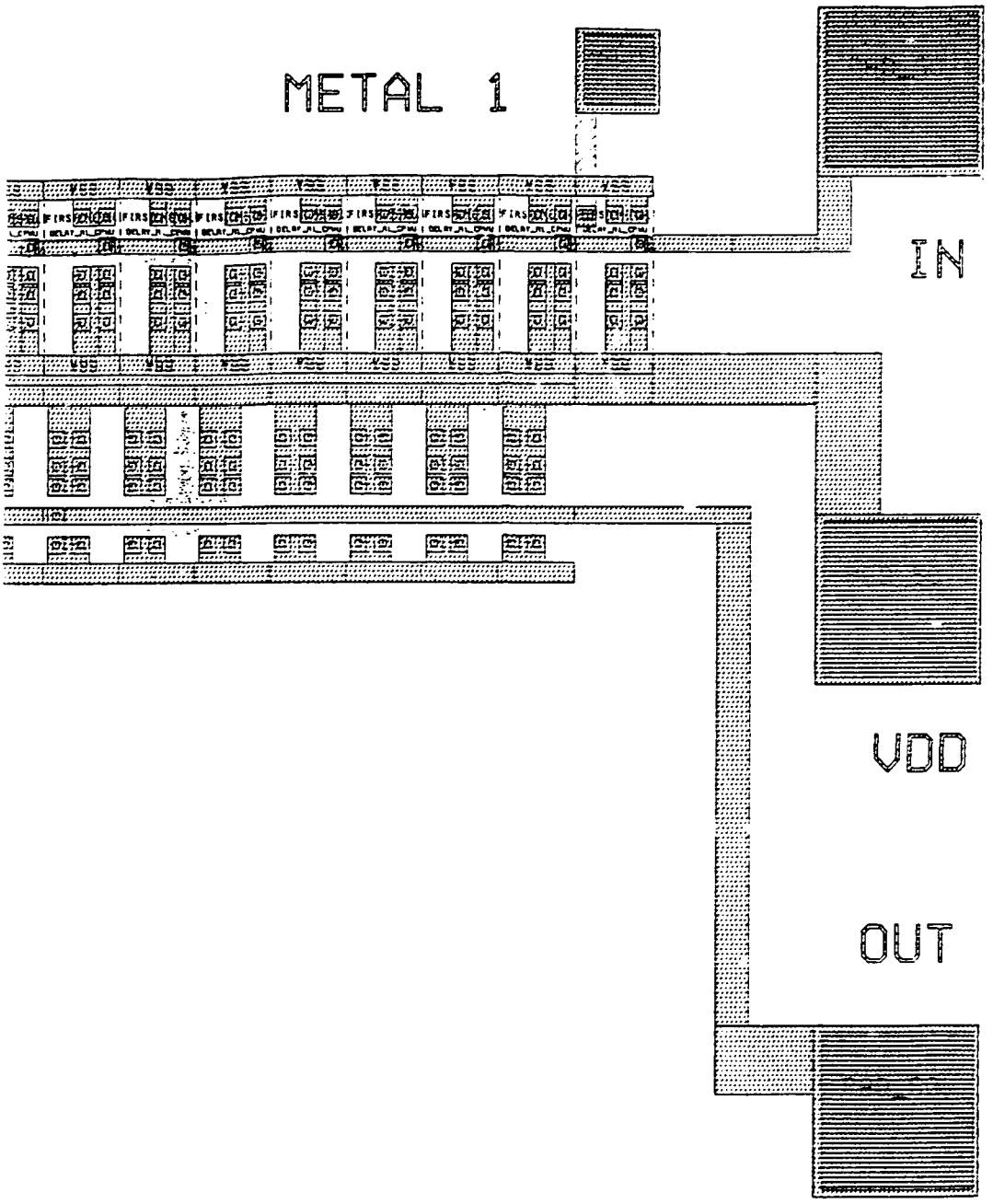


Figure 9. Layout drawing (with portions omitted) of the sacrificial metal mask with all the gates connected for voltage stressing.

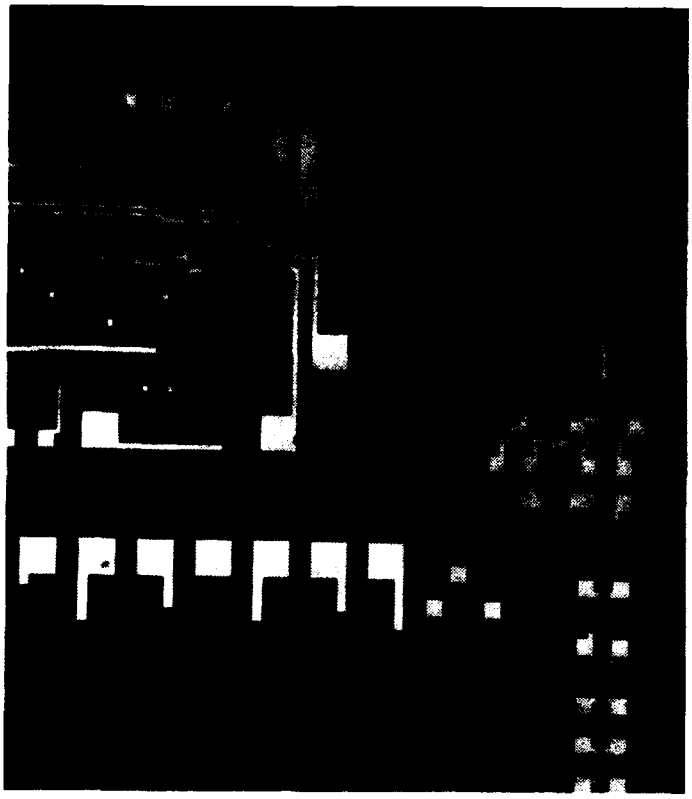


Figure 10. Photomicrograph of the GEM WAT key showing the 101-stage Metal-1 Delay Line circuit and POLY CAP on p-well and POLY CAP on n-well structures.

5.4 The Experiment

5.4.1 Description

An experiment involving routine process lots in Sarnoff's IC Center was performed to investigate the merit and side effects of in-process oxide screening on the reliability of the gate oxide and the extra processing steps on the product yield. Two lots of BiCMOS GEM wafers were processed, with each lot having a 3-way split. In the first lot of 18 wafers, devices were fabricated with normal gate oxide thickness of 240Å. The first split group of 6 wafers (C1 to C6) were control wafers, with neither the sacrificial metallization nor in-process voltage stress. The second group of 6 wafers (K1 to K6) were control wafers with the sacrificial metallization but no in-process voltage stress. The third group of 6 wafers (T1 to T6) were test wafers with sacrificial metallization and in-process voltage stress. The experimental test consisted of the following sequence of steps, which are shown schematically in Fig. 11.

1. The VROB measurements were performed at 1 V/s on wafer C1, C2, C3 and C4, with negative polarity on the polysilicon electrode, using test structures POLY CAP on p-well. Wafer C1 was tested at 55°C in the upper half of the wafer, and at 80°C in the lower half. Similarly, wafer C2 was tested at 125°C and at 200°C. Wafers C3 and C4 were tested at 125°C. TDDB measurements on wafers C5 and C6 were performed at 125°C, using test structures POLY CAP on p-well. The in-process screen voltage (using a voltage-ramp method) was then chosen at 3 V less than the median breakdown voltage for intrinsic or inherent breakdown. The above procedure with reversed polarity was repeated for POLY CAP on n-well.

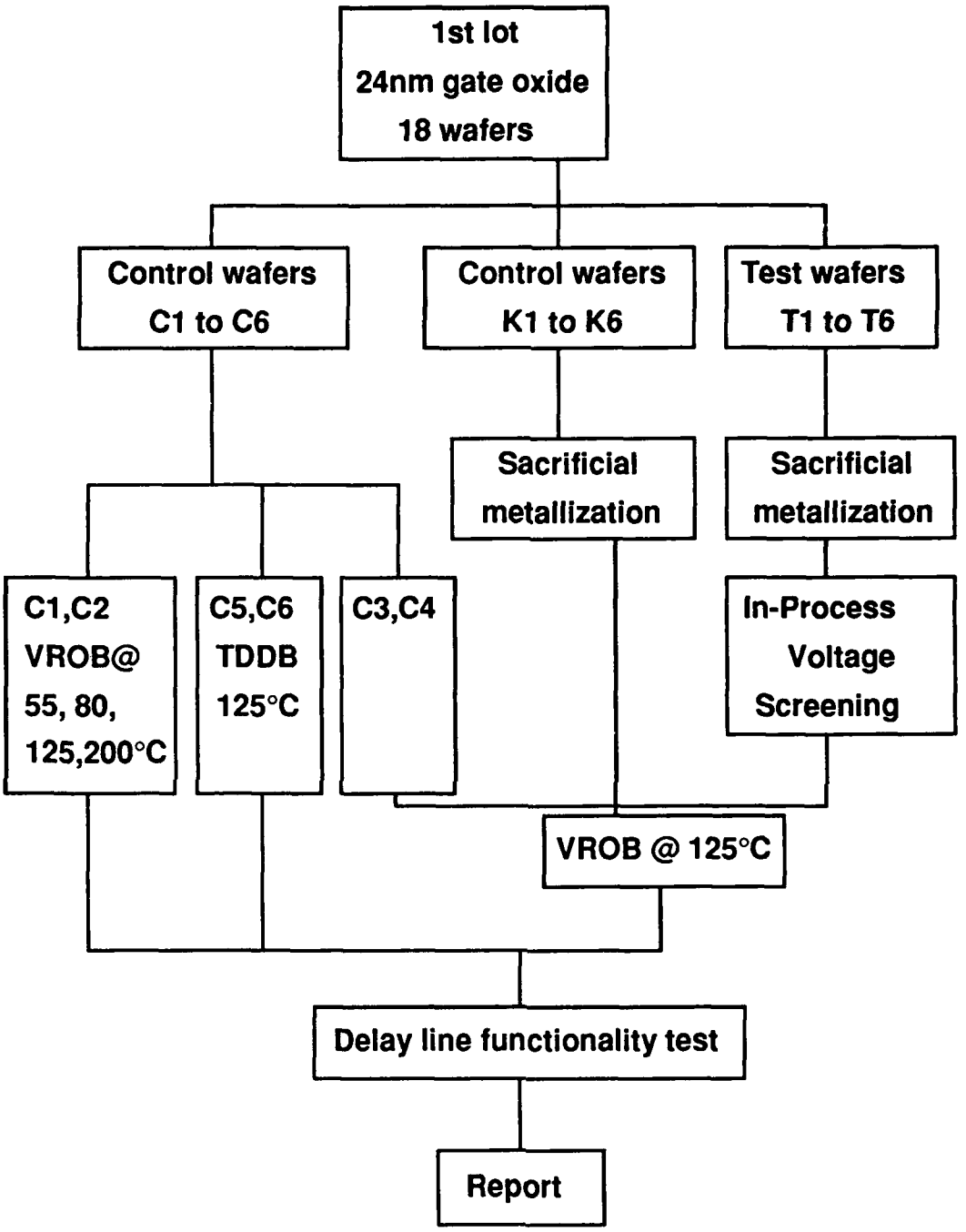
2. For wafers T1 to T6, in-process voltage stress was applied at 125°C to p-well polysilicon capacitors, n-well polysilicon capacitors, and Metal-1 Delay Lines. For p-well polysilicon capacitors, the polysilicon electrode was biased negative with respect to the p-well. For n-well polysilicon capacitors, the polysilicon electrode was biased positive with respect to the n-well. For the Metal-1 Delay Line, the gates were biased first positively and then negatively with respect to the V_{DD} and V_{SS} lines, thus fully stressing the gate oxides in both p-channel and n-channel transistors. Records were kept on all devices and circuits that failed during in-process voltage stressing.

3. Sacrificial metallization was removed from all wafers (K1 to K6, T1 to T6). Wafers K1 to K6 were not voltage stressed but were metallized with the same sacrificial metal pattern to serve as controls.

4. Wafers K1 to K6 and T1 to T6 were metallized and patterned with First-Level Metallization Mask. Metal contact resistances were measured in test patterns in these wafers after the First Level Metallization and compared to values measured before the removal of the sacrificial metallization.

5. The VROB measurements were performed on wafers K1 to K6 and T1 to T6 at 125°C, using the p-well and n-well polysilicon capacitors with the proper polarity.

6. The Metal-1 Delay Lines in wafers C1 to C6, K1 to K6 and T1 to T6 were tested for device functionality as a monitor for the effect of extra processing steps on circuit yield. Testing was performed with square pulses of 50 μs pulse-width and 5 V amplitude as inputs, and output waveforms were monitored on an oscilloscope. In addition, I_{DD} currents were monitored and recorded during device switchings.



Repeat with 2nd lot of 18 wafers with 15nm gate oxide.

Figure 11. Flow diagram of the split-lot experiments to investigate the effect on in-process oxide screening the circuit yield and reliability.

In the second lot of wafers, the standard GEM process used in the first lot was altered to weaken the gate oxide. The gate oxide thickness was changed to 150Å instead of 240Å. This should enhance the probability of observing oxide failures in test devices and circuits not given the in-process voltage stress and, therefore, increase the sensitivity of the evaluation of the in-process screen. The same test procedures as outlined above was used on the second lot wafers and the results analyzed

Testing was performed on a HP4062C Semiconductor Parametric Analyzer which automatically performs step and repeat measurements on each die on a wafer under test. Software was specifically developed for the VROB, the TDDB measurements and the in-process voltage stressing of the gate oxides in the 101-stage delay-line circuit and the polysilicon capacitors over n-well and p-well. A listing of the software programs are given in Appendices B and C.

Lastly, failure analysis was performed on selected devices that failed during screening or during the life tests to verify which were caused by oxide breakdowns in order to assess screening effectiveness. Failure analysis included selectively removing the overlying layers of the devices and etching the samples in defect-revealing etchants.

5.4.2 Results of split-lot experiment

5.4.2.1 Results of in-process voltage screen on first test lot

Control wafers C1 and C2 were characterized with respect to VROB tests. The VROB measurements were performed at 1 V/s, using test structures POLY CAP on n-well biased in accumulation. Wafer C1 was tested at 55°C in the upper half on the wafer, and at 80°C in the lower half. Except for one die located near the wafer edge in each case with a visually obvious photolithographic problem, there was no pre-mature oxide breakdown observed. Wafer C2 was tested at 125°C and at 200°C, and only one pre-mature breakdown was observed in each case. Based on the data from wafers C1 and C2, a decision was made to test the rest of the wafers at 125°C in an attempt to enhance failures in the samples, since very low defect density in the gate oxide up to level-1 metallization in the BiCMOS GEM wafers could present a problem for a clear demonstration of the effectiveness of the in-process oxide screening experiment. Figure 12 shows an example of measured and stored VROB data for POLY CAP on n-well and POLY CAP on p-well. The breakdown voltage V_{BD} where currents exceed 50 mA are stored as well as the entire I-V characteristics for each chip on a test wafer so that each device can be subsequently analyzed in greater details if needed.

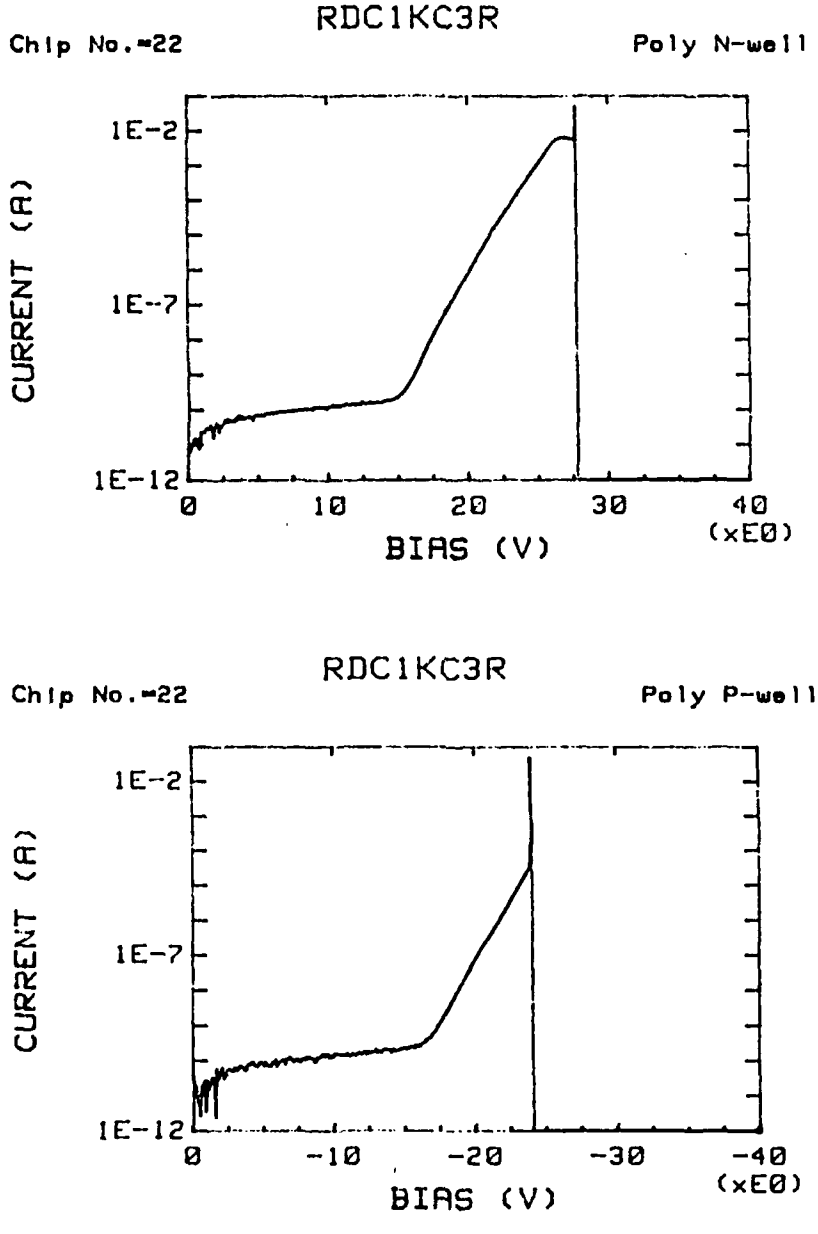


Figure 12. An example of measured and stored VROB data.

Control wafers C3 and C4 were characterized with respect to VROB tests at 125°C and at 1 V/s, using test structures POLY CAP on n-well biased in accumulation. The median breakdown voltage for intrinsic breakdown was found to be 27.6 V, and the in-process screening voltage was then chosen at 24.6 V. For test structures POLY CAP on p-well, biased with negative polarity on the polysilicon electrode, the median breakdown voltage for intrinsic breakdown was found to be -27.6 V, and the in-process screening was chosen at -24.6 V. This choice of screening voltage gives, according to Eq.(20), $\Delta_S = 4.4\%$ for the percentage of damage to the good devices incurred during screening.

In-process voltage stress was applied at 125°C to p-well polysilicon capacitors, n-well polysilicon capacitors and Metal-1 Delay Lines in test wafers T1 to T6. The screening voltages were 24.6 V applied at 1 V/s for n-well capacitors, and -24.6 V for p-well capacitors, respectively. For the Metal-1 Delay Lines, the gates (which were connected together with a sacrificial metal pattern) were biased first positively and then negatively with respect to the V_{DD} and V_{SS} lines, thus fully stressing the gates in both p-channel and n-channel transistors. Records were kept on all devices that failed during the in-process voltage stressing. Wafers T1 to T6, together with wafers K1 to K6 (which were not voltage stressed but were metallized with the same sacrificial metal pattern), were wet-etched to remove the sacrificial metallization, and then re-metallized and patterned with the First-Level Metallization for the final evaluation of the effects of the in-process oxide screening. Wet-etching was chosen to remove the sacrificial metallization instead of dry etching to avoid any radiation damage to the oxide layer. Table 3 summarizes the results of the experiment for the GEM lot with 240Å gate oxide. It can be seen from the data that the effect of patterning and removal of the sacrificial metallization increased the cumulative percent failure of gate oxide for large-area capacitors from 0.8% to 2.3%, as determined by VROB tests, and that screening of gate oxide for large-area capacitors using a sacrificial metallization completely eliminated the defective population.

Results of delay line functionality tests are summarized in Table 4. For delay lines, there was a slight adverse effect on circuit yield, increasing initial percent of failures from 6.8% to 7.2%, due to patterning and removal of the sacrificial metallization. In-process voltage screening of gate oxides for the 101-stage delay-lines using sacrificial metallization was found to improve circuit yield, with initial percent of failures decreasing from 6.8% to 3.4%. This should be contrasted with the complete elimination of the defective population in the case of voltage screening of gate oxide using a

similar sacrificial metallization for large-area capacitors which are much simpler devices to fabricate, indicating the probable existence of other factors not addressed by the gate oxide screening, such as photolithography, etching uniformity, implant uniformity and contaminations, etc.

Table 3. Results of VROB tests for large-area capacitors with 240Å oxide layers.

Wafers	Units tested	Units failed	Percentage failure
C3,C4	124	1	0.8±0.8%
K1,K2,K3,K4,K5,K6	306	7	2.3±0.9%
T2,T3,T4	181	0	0.0±0.6%

Table 4. Results of Metal-1 Delay Line functionality tests for devices with 240Å gate oxides.

Wafers	Units tested	Units failed	Percentage failure
C5,C6	44	3	6.8±3.9%
K1,K3,K4,K5,K6	153	11	7.2±2.2%
T2,T4,T5	89	3	3.4±2.0%

The effect of extra processing steps used to pattern and remove the sacrificial metallization on the metal-polysilicon contact resistance was also investigated. Regular WAT tests were performed on a control wafer C4 (Wafer No. 4) and on a test wafer T3 (Wafer No.15) after the wet-etching removal of the sacrificial metallization and the re-metallization and patterning with the First-Level Metallization. The results of the WAT tests, which include many useful data for BiCMOS circuits, are given in Tables 5 and 6. The metal-polysilicon contact resistance for 2 μm x 2 μm openings were 6.50 ± 0.35 ohms for control wafers and 6.39 ± 0.28 ohms for test wafers, respectively. For 3 μm x 3 μm openings, the contact resistances were 4.16 ± 0.17 ohms for control wafers and 4.10 ± 0.17 ohms for test wafers, respectively. Thus, no adverse effect was found on the metal-

Table 5. The WAT test results on control wafer C4 (Wafer No. 4) after First-Level Metallization.

	WAT PARAMETER	SPEC	OB	OK	MEDIAN	MEAN	SIGMA	MIN	MAX
NMOS	Gate Leakage	< 100 pA	32	32	1.90E-11	2.33E-11	1.47E-11	1.18E-11	3.65E-11
	Idleak @Vds = 5V	< 100 pA	32	31	1.90E-11	1.98E-11	4.73E-12	1.60E-11	2.45E-11
	Idrive W = 10µm	> 2.0 mA	32	30	2.45E-03	2.43E-03	5.00E-05	2.39E-03	2.47E-03
	Vtn	.8 ±0.2	32	31	0.78	0.78	0.01	0.77	0.792
	BVds @10µA	> 12.0 V	32	31	13.77	13.75	0.47	13.47	14.150
PMOS	Gate Leakage	> -100 pA	32	32	-3.90E-11	-4.68E-11	2.11E-11	-6.63E-11	-3.00E-11
	Idleak @Vds = -5V	> -100 pA	32	32	-2.10E-11	-2.28E-11	5.78E-12	-2.90E-11	-1.80E-11
	Idrive W = 20µm	< -2.0 mA	32	29	-2.23E-03	-2.22E-03	5.72E-05	-2.25E-03	-2.20E-03
	Vtn	-1.0 ±0.2	32	32	-1.01	-1.02	0.02	-1.03	-1.004
	BVsd @10µA	< -12.0 V	32	27	-14.05	-14.05	0.05	-14.09	-14.010
P-Field	Vtfn	< -9.0 V	32	32	-11.41	-11.46	0.11	-11.54	-11.380
NPN	BVceo	> 12.0 V	32	26	12.18	12.45	4.49	8.13	16.950
	ßeta @Ic = 50µA	ßeta > 50	31	31	88.50	95.11	25.13	79.13	113.100
	ßeta @Ic = 1mA	ßeta > 40	31	31	83.48	88.39	20.36	75.24	104.300
ZENER	Vbkdn @1.0µA	6.0 ±0.3	32	31	5.640	5.641	0.023	5.624	5.657
	Vbkdn @1.0mA	6.0 ±0.3	32	31	5.810	5.804	0.031	5.771	5.834
N-Plus	N-Plus Rc 2.0µm	< 40	32	31	37.25	38.07	4.71	34.63	40.380
	N-Plus Rc 3.0µm	< 20	32	30	19.25	19.49	2.30	17.56	20.940
	N-Plus Rs (ohms/sq)	40 ± 8	32	31	32.38	32.43	0.19	32.28	32.540
P-Plus	P-Plus Rc 2.0µm	< 30	32	31	14.00	13.84	0.55	13.37	14.250
	P-Plus Rc 3.0µm	< 20	32	31	9.00	8.98	0.31	8.75	9.250
	P-Plus Rs (ohms/sq)	85 ± 15	32	31	58.77	58.60	1.42	57.50	59.610
POLY	Poly Rc 2.0µm	< 10	32	31	6.50	6.50	0.35	6.25	6.750
	Poly Rc 3.0µm	< 5	32	29	4.25	4.16	0.17	4.00	4.250
	Poly DW	0.5 ± 0.3	32	30	0.485	0.491	0.028	0.469	0.509
	Poly Rs (ohms/sq)	17.5 ± 2.5	32	31	17.08	16.99	0.38	16.77	17.220
P-Base	P-Base Rs (ohms/sq)	700 ±100	32	32	691.10	694.10	21.85	680.40	712.900

Constant voltage TDDB measurements at 125°C were performed on large-area capacitors on wafers C5 and C6, and the results are shown in Fig.13. These measured TDDB distributions are then compared to VROB distributions obtained for wafers C3 and C4 in the same control group. This is accomplished by transforming the results of VROB distributions to TDDB distributions, using Eq. (16) which gives the relation between V_{BD} of a ramp voltage test at temperature T_t and t_{BD} of a constant voltage V_{OX} test at T_t. Figure 14 shows the results of the TDDB distributions derived from VROB distributions. There is only fair agreement with the measured TDDB distributions for similar devices in the same control group. Both methods give similar percentage of defective populations, but the spreads in the good devices are much tighter when similar devices are measured with the VROB technique.

Table 6. The WAT test results on test wafer T3 (Wafer No.15) after wet-etching removal of Sacrificial Metallization and re-metallization with First-Level Metallization.

	WAT PARAMETER	SPEC	OB	OK	MEDIAN	MEAN	SIGMA	MIN	MAX
NMOS	Gate Leakage	< 100 pA	32	31	9.20E-11	1.18E-10	6.99E-11	6.25E-11	1.68E-10
	Idleak @Vds = 5V	< 100 pA	32	31	3.90E-11	3.85E-11	9.39E-12	2.95E-11	4.55E-11
	Idrive W = 10µm	> 2.0 mA	32	30	2.41E-03	2.40E-03	3.94E-05	2.38E-03	2.42E-03
	Vtn	0.8 ±0.2	31	31	0.78	0.78	0.01	0.77	0.792
	BVds @10µA	> 12.0 V	31	29	13.70	13.69	0.26	13.61	13.840
PMOS	Gate Leakage	> -100 pA	32	31	-1.80E-10	-1.91E-10	8.82E-11	-2.46E-10	-1.19E-10
	Idleak @Vds = -5V	> -100 pA	32	30	-4.50E-11	-4.73E-11	1.03E-11	-5.63E-11	-3.30E-11
	Idrive W = 20µm	< -2.0 mA	32	30	-2.06E-03	-2.06E-03	4.47E-05	-2.10E-03	-2.03E-03
	Vtn	-1.0 ±0.2	32	32	-1.01	-1.01	0.02	-1.02	-0.998
	BVsd @10µA	< -12.0 V	32	30	-13.55	-13.56	0.05	-13.59	-13.510
P-Field	Vtfn	< -9.0 V	31	28	-11.30	-11.35	0.15	-11.43	-11.250
NPN	BVceo	> 12.0 V	32	28	16.76	16.77	1.00	16.06	17.390
	ßeta @Ic = 50µA	ßeta > 50	31	31	79.94	84.32	22.24	67.07	104.000
	ßeta @Ic = 1mA	ßeta > 40	31	31	73.52	77.23	18.31	63.28	93.380
ZENER	Vbkdn @1.0µA	6.0 ±0.3	32	29	5.650	5.649	0.010	5.640	5.655
	Vbkdn @1.0mA	6.0 ±0.3	32	31	5.855	5.862	0.028	5.840	5.885
N-Plus	N-Plus Rc 2.0µm	< 30	32	31	21.50	22.20	2.01	20.88	23.250
	N-Plus Rc 3.0µm	< 20	32	31	12.00	12.53	1.12	11.75	13.250
	N-Plus Rs (ohms/sq)	40 ± 8	32	31	33.74	33.77	0.23	33.61	33.920
P-Plus	P-Plus Rc 2.0µm	< 30	32	31	12.75	12.66	0.48	12.25	13.000
	P-Plus Rc 3.0µm	< 20	32	31	8.25	8.35	0.31	8.13	8.500
	P-Plus Rs (ohms/sq)	85 ± 15	32	31	63.56	63.47	1.48	62.36	64.590
POLY	Poly Rc 2.0µm	< 10	32	30	6.50	6.39	0.28	6.25	6.500
	Poly Rc 3.0µm	< 5	32	32	4.13	4.10	0.17	4.00	4.250
	Poly DW	0.5 ±0.3	32	29	0.478	0.472	0.023	0.464	0.487
	Poly Rs (ohms/sq)	17.5 ± 2.5	32	32	16.98	16.89	0.48	16.61	17.220
P-Base	P-Base Rs (ohms/sq)	700 ±100	32	31	704.00	698.30	25.65	679.30	720.600

5.4.2.2 Results of in-process voltage screen on second test lot

Control wafers C'1, C'2, C'3 and C'4 were characterized with respect to VROB tests at 125°C and at 1 V/s. The median breakdown voltage for intrinsic breakdown was found to be 20.2 V for POLY CAP on n-well, and -20.5 V for POLY CAP on p-well. The in-process screening voltages chosen were 17.2 V for POLY CAP on n-well and -17.5 V for POLY CAP on p-well, respectively. This choice of screening voltage gives, according to Eq. (20), $\Delta_S \sim 1\%$ as the percentage of damage to the good devices incurred during the in-process oxide screening. As before, records were kept on all devices and circuits that failed during the in-process voltage stressing of the test capacitors and the delay line circuits, as well as all subsequent VROB tests

and circuits that failed during the in-process voltage stressing of the test capacitors and the delay line circuits, as well as all subsequent VROB tests to characterize the gate oxides, and the circuit functionality tests. The results of the experiment for the GEM lot with 140Å gate oxide are summarized in Table 7 for the oxide characterization tests. From the data, the effect of patterning and removal of the sacrificial metallization was found to have no adverse effect on the cumulative percent failure of gate oxide for large-area capacitors, which remained at 4.4% as determined by VROB tests. Voltage screening of gate oxide for large-area capacitors using a sacrificial metallization completely eliminated the infant mortality portion of the defective population. The cumulative percent failure of gate oxide for large-area capacitors was decreased from 4.8% to <1%. A closer examination of the 1% of the capacitors that failed after in-process screening revealed that their breakdown voltages were very close to the screening voltages used which were quite high (17.2V for capacitors on n-well and -17.5 V for capacitors on p-well, respectively) and, therefore, represented units that would function satisfactorily in field usage [56].

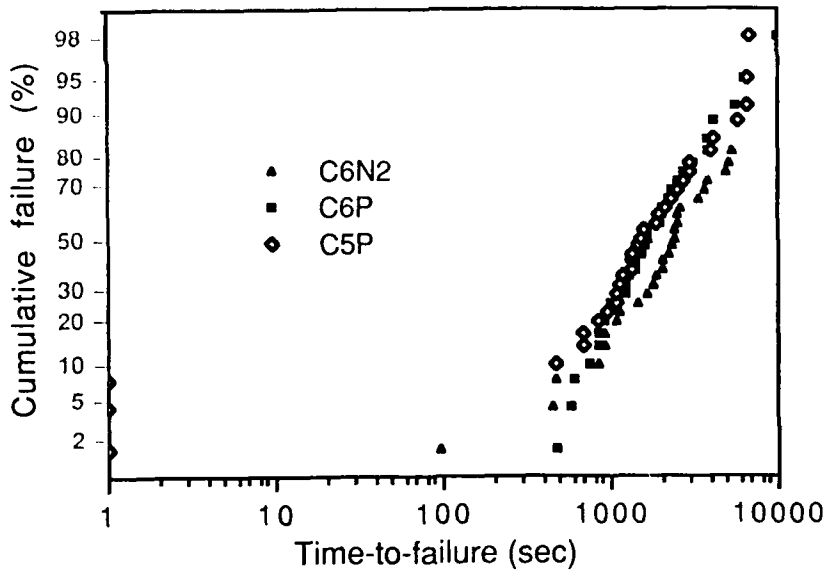


Figure 13. Measured TDDB distributions at 125°C and $|V_t|$ = 22.5V for polysilicon capacitors on wafers C5 and C6.

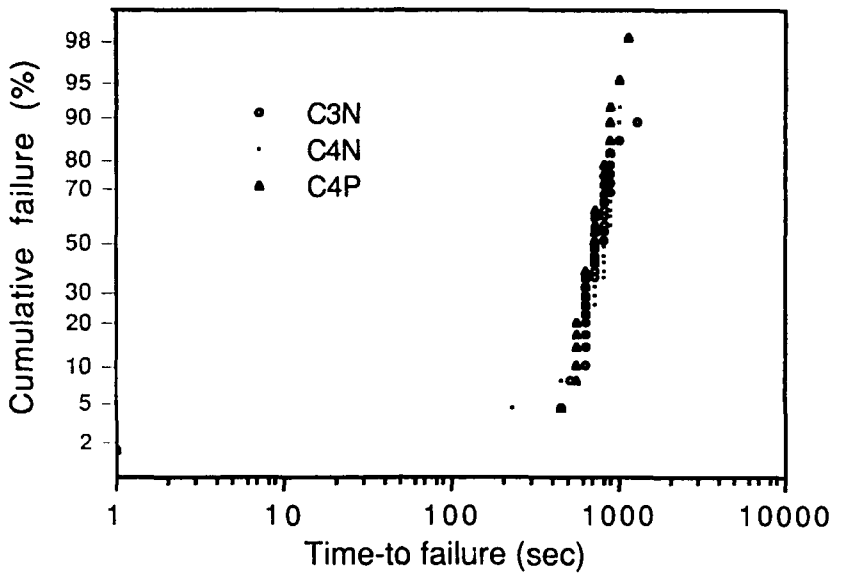


Figure 14. The TDDB distributions derived from VROB distributions at 125°C for wafers C3 and C4.

Results of delay-line functionality tests for the GEM lot with 140Å gate oxide are summarized in Table 8. Analysis of the device functionality test results showed that there was no adverse effect on circuit yield due to patterning and removal of the sacrificial metallization (the results of the second lot actually indicated an improvement, but the combined results of the two lots showed that the delay-line circuit yield with the extra processing steps was 4.3±1.1% as compared to 4.4±1.4% for the controls), and that voltage screening of the gate oxides for the 101-stage delay lines using sacrificial metallization decreased the cumulative percent failure from 3.0% to 1.7%. This result, as in the first lot of GEM wafers with 250Å gate oxide, indicated the existence of other factors not addressed by gate oxide screening.

Tables 9 and 10 show the results of WAT tests for the second lot of GEM wafers. The metal-polysilicon contact resistances for 2 μm x 2 μm openings were 8.28 ± 0.51 ohms for control wafers and 8.23 ± 0.30 ohms for test wafers which were re-metallized after the wet etching and removal of the sacrificial metallization pattern. For 3 μm x 3 μm openings, the contact resistances were 5.09 ± 0.36 ohms for control wafers and 4.93 ± 0.22 ohms for test wafers, respectively. Again, no adverse effect was found on the metal-polysilicon contact resistance due to patterning and removal of the sacrificial metallization used to voltage screen gate oxides.

Table 7. Results of VROB tests for large-area capacitors with 150Å oxide layers.

Wafers	Units tested	Units failed	Percentage failure
C'1,C'2,C'3,C'4	250	12	4.8±1.4%
K'1,K'2,K'3,K'4,K'5,K'6	383	17	4.4±1.1%
T'1,T'2,T'3,T'4,T'5,T'6	365	3	0.8±0.5%

Table 8. Results of Metal-1 Delay Line functionality tests for devices with 150Å gate oxides.

Wafers	Units tested	Units failed	Percentage failure
C'1,C'2,C'3,C'4,C'5,C'6	184	7	3.8±1.4%
K'1,K'2,K'3,K'4,K'5,K'6	174	3	1.7±1.0%
T'1,T'2,T'3,T'4,T'5,T'6	182	4	2.2±2.0%

Figure 15 shows the measured constant voltage TDDB distributions at 125°C for large-area capacitors on wafers C'5 and C'6. Quite similar TDDB distributions are derived from VROB distributions for wafers C'2 and C'4 in the same control group and these are shown in Fig. 16. In particular, both methods of measurement give similar percentage of defective populations and similar order of magnitude for time-to-failures for similar wafers. This correlation between TDDB measurements and VROB measurements allows us to use the VROB tests as reliability life tests for thin oxide layers, as stipulated by the reciprocal field model for oxide breakdowns.

Table 9. The WAT test results on control wafer C'5 (Wafer No. 25) after First-Level Metallization.

	WAT PARAMETER	SPEC	OB	OK	MEDIAN	MEAN	SIGMA	MIN	MAX
NMOS	Gate Leakage	< 100 pA	32	31	-1.00E-12	4.52E-13	3.43E-12	-2.00E-12	3.00E-12
	Idleak @Vds = 5V	< 100 pA	32	29	2.30E-11	2.28E-11	3.00E-12	2.10E-11	2.40E-11
	Idrive W = 10•m	> 3.0 mA	32	31	3.25E-03	3.21E-03	1.38E-04	3.13E-03	3.31E-03
	Vtn	0.5 +/-0.2	32	28	0.49	0.49	0.01	0.48	0.493
	BVds @10•A	> 12.0 V	32	32	13.29	12.95	0.94	12.64	13.720
PMOS	Gate Leakage	> -100 pA	32	32	-1.10E-11	-1.30E-11	3.75E-12	-1.60E-11	-1.00E-11
	Idleak @Vds = -5V	> -100 pA	32	28	-1.55E-11	-1.63E-11	2.55E-12	-1.73E-11	-1.48E-11
	Idrive W = 20•m	< -2.0 mA	32	30	-2.48E-03	-2.50E-03	1.07E-04	-2.56E-03	-2.44E-03
	Vtp	-1.0 +/-0.2	32	32	-0.97	-0.96	0.04	-0.98	-0.929
	BVsd @10•A	< -12.0 V	32	30	-12.20	-12.18	0.04	-12.22	-12.140
NPN	BVceo	> 12.0 V	32	32	13.16	10.85	4.43	7.42	14.690
	ßeta @Ic = 50•A	ßeta > 50	32	32	92.73	92.07	21.38	76.00	103.800
	ßeta @Ic = 1mA	ßeta > 40	32	32	85.66	84.59	17.80	70.80	93.900
ZENER	Vbkdn @1.0•A	6.0 +/-0.3	32	30	5.892	5.893	0.020	5.875	5.907
	Vbkdn @1.0mA	6.0 +/-0.3	32	31	6.065	6.069	0.029	6.045	6.091
N-Plus	N-Plus Rc 2.0•m	< 40	32	29	42.50	43.99	4.20	41.50	45.250
	N-Plus Rc 3.0•m	< 30	32	31	21.00	21.49	1.61	20.25	22.500
	N-Plus Rs (ohms/sq)	34 +/- 5	32	32	31.39	31.37	0.27	31.18	31.560
P-Plus	P-Plus Rc 2.0•m	< 30	32	30	17.63	17.60	0.47	17.25	18.000
	P-Plus Rc 3.0•m	< 20	32	32	11.50	11.45	0.40	11.00	11.750
	P-Plus Rs (ohms/sq)	75 +/- 10	32	31	67.30	67.02	1.32	66.14	67.960
POLY	Poly Rc 2.0•m	< 10	32	29	8.25	8.28	0.51	7.75	8.750
	Poly Rc 3.0•m	< 5	32	31	5.00	5.09	0.36	4.75	5.250
	Poly Rs (ohms/sq)	16.5 +/-2.5	32	32	16.44	16.38	0.53	15.92	16.890
P-Base	P-Base Rs (ohms/sq)	700 +/-50	32	32	663.50	655.80	20.16	637.30	670.400

Table 10. The WAT test results on test wafer T'7 (Wafer No.40) after wet-etching removal of Sacrificial Metallization and re-metallization with First-Level Metallization.

	WAT PARAMETER	SPEC	OB	OK	MEDIAN	MEAN	SIGMA	MIN	MAX
NMOS	Gate Leakage	< 100 pA	32	28	-5.00E-12	-5.32E-12	7.23E-13	-6.00E-12	-5.00E-12
	Idleak @Vds = 5V	< 100 pA	32	29	2.30E-11	2.38E-11	3.71E-12	2.20E-11	2.70E-11
	Idrive W = 10•m	> 3.0 mA	32	31	3.06E-03	3.03E-03	1.49E-04	2.95E-03	3.14E-03
	Vtn	0.5 +/-0.2	32	31	0.49	0.49	0.01	0.48	0.494
	BVds @10•A	> 12.0 V	32	32	13.28	12.78	1.17	11.86	13.760
PMOS	Gate Leakage	> -100 pA	32	25	-8.00E-12	-8.00E-12	0.00E+00	-8.00E-12	-8.00E-12
	Idleak @Vds = -5V	> -100 pA	32	30	-1.40E-11	-1.61E-11	3.87E-12	-1.80E-11	-1.30E-11
	Idrive W = 20•m	< -2.0 mA	32	31	-2.30E-03	-2.33E-03	1.29E-04	-2.44E-03	-2.22E-03
	Vtp	-1.0 +/-0.2	32	31	-0.96	-0.95	0.03	-0.98	-0.917
	BVsd @10•A	< -12.0 V	32	31	-12.17	-12.16	0.06	-12.21	-12.130
NPN	BVceo	> 12.0 V	32	32	12.35	9.82	4.65	7.24	13.810
	ßeta @Ic = 50•A	ßeta > 50	31	31	90.12	89.27	16.83	79.04	100.800
	ßeta @Ic = 1mA	ßeta > 40	31	31	82.99	81.87	14.15	72.31	91.500
ZENER	Vbkdn @1.0•A	6.0 +/-0.3	32	31	5.875	5.873	0.023	5.855	5.892
	Vbkdn @1.0mA	6.0 +/-0.3	32	31	6.070	6.078	0.026	6.057	6.096
N-Plus	N-Plus Rc 2.0•m	< 40	32	31	42.75	43.41	2.37	42.00	45.130
	N-Plus Rc 3.0•m	< 30	32	32	22.00	22.12	1.14	21.25	23.000
	N-Plus Rs (ohms/sq)	34 +/- 5	32	29	31.79	31.76	0.17	31.65	31.850
P-Plus	P-Plus Rc 2.0•m	< 30	32	32	18.00	18.03	0.55	17.50	18.500
	P-Plus Rc 3.0•m	< 20	32	31	11.75	11.76	0.41	11.50	12.000
	P-Plus Rs (ohms/sq)	75 +/- 10	32	31	70.77	70.57	0.99	70.00	71.380
POLY	Poly Rc 2.0•m	< 10	32	24	8.00	8.23	0.30	8.00	8.500
	Poly Rc 3.0•m	< 5	32	30	5.00	4.93	0.22	4.75	5.000
	Poly Rs (ohms/sq)	16.5 +/-2.5	32	32	16.54	16.46	0.53	16.07	16.910
P-Base	P-Base Rs (ohms/sq)	700 +/-50	32	32	668.50	659.50	19.85	647.20	674.500

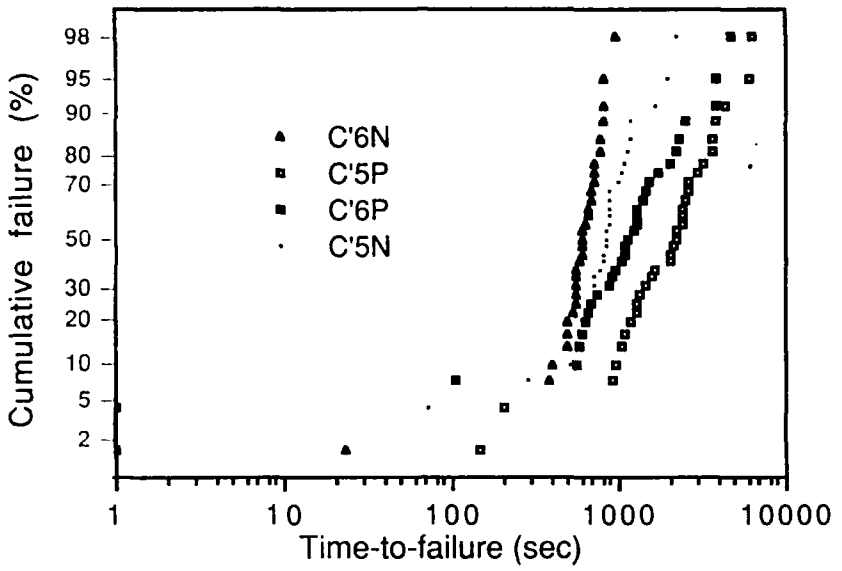


Figure 15. Measured TDDB distributions at 125°C for polysilicon capacitors on wafers C'5 and C'6.

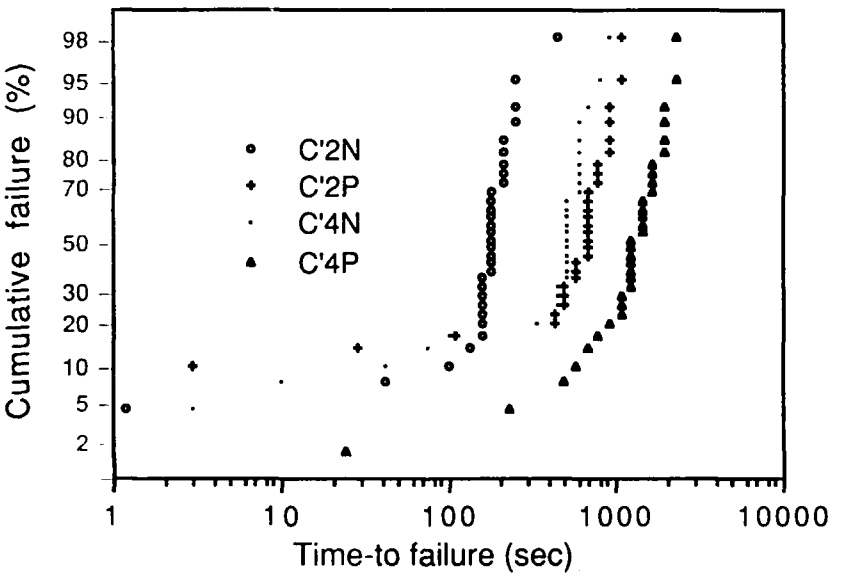


Figure 16. The TDDB distributions derived from VROB distributions at 125°C for wafers C'2 and C'4.

5.5 Failure Analysis

Failure analysis was performed on failed devices and circuits to determine the location and type of failure mechanism. In most cases, device or circuit failure could be obviously attributed to causes other than gate oxide failures, such as photolithographic problems for units at the edge of the wafers, metallization or etching problems, and scratches. These devices or circuits were not counted. Failed devices and circuits that passed cosmetic inspection under a Normaski microscope were then subjected to more analysis by selectively removing the Al metallization in H_3PO_4 at 70°C, and the polysilicon layer in aqueous HF-HNO_3 (1:100) solution and etching the samples in aqueous sodium metasilicate at 70°C to reveal pinholes in the gate oxide and/or in "Wright" etch to reveal any defects in the silicon substrate. Since all polysilicon capacitors were ramp-voltage tested to failure before the failure analysis, all capacitors showed what appeared to be a short, as shown in Fig. 17 which is a scanning electron microscopy (SEM) photograph of a defect in the capacitor on die T4-1. Thus, failure analysis performed on failed capacitors had only very limited values since one could not be certain whether or not the observed defect was what actually caused the pre-mature dielectric breakdown. The delay lines, however, were not voltage-ramped to failure, and the failure analysis used was very successful in identifying those units that failed functionality test because of gate oxide defects. Two examples are shown in Figs. 18 and 19 which are SEM photographs of shorted gates on control wafer K1.

As with the first lot of GEM test wafers, failure analysis was performed on failed devices and circuits to determine the location and type of failure mechanisms to eliminate from the final analysis those failures that obviously were not related to gate oxide failures, and probable failure sites were located on 8 of the 17 capacitors and on all 8 delay-line structures examined.

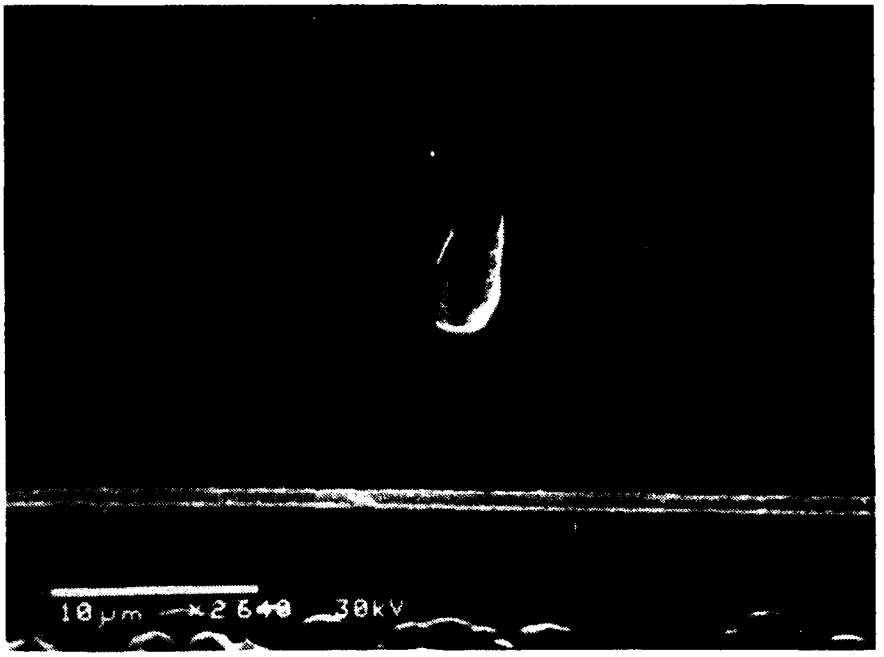


Figure 17. An SEM photograph showing location of a defect in capacitor dielectric on die T4-1.

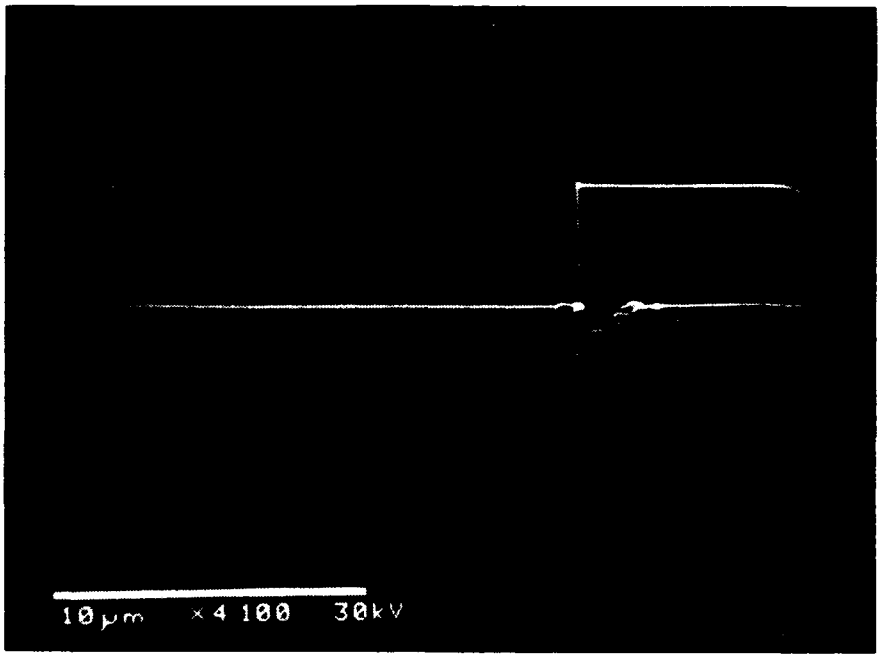


Figure 18. An SEM photograph showing shorted gate on die K1-25.

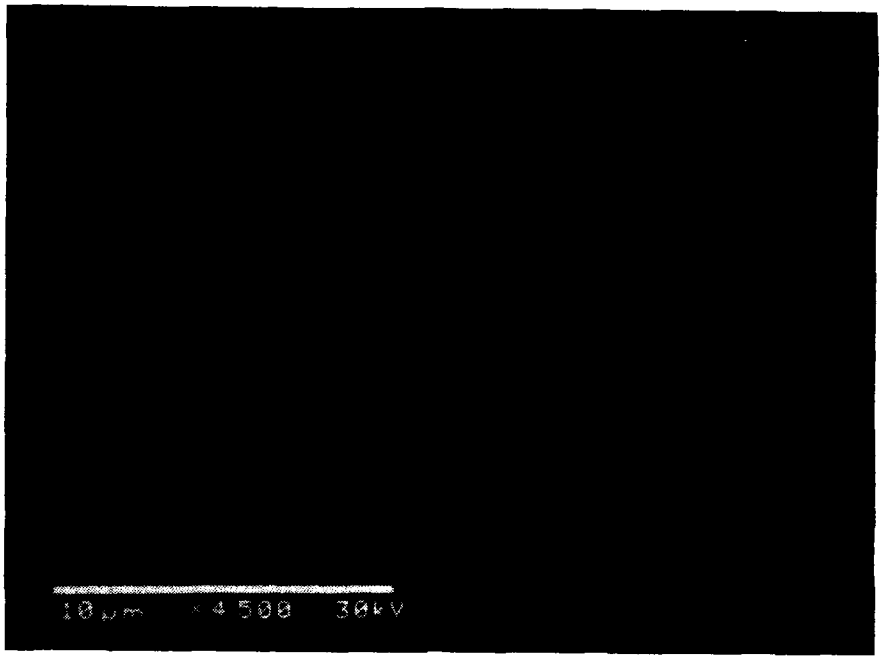


Figure 19. An SEM photograph showing shorted gate on die K1-30.

6. CONCLUSIONS

Time-dependent dielectric breakdown of gate oxide is one of the principal failure mechanisms of MOS ICs, and voltage stressing of completed devices to screen oxide defects is ineffective with high-density MOS ICs due to the limitation in the voltage that can be applied to all the gates and the inability to stress all oxides equally.

Through a literature search of approximately 200 references, the sacrificial metal pattern technique is found to be the best approach to 100% in-process oxide reliability screening since it can be applied near the end in the wafer process sequence, after all high-temperature processing steps, ion implantations and most, if not all, of plasma etching steps. The sacrificial metal pattern technique for in-process oxide screening gives 100% coverage and even oxide stressing with little or no adverse effect on circuit performance. It is also simple to implement in bulk CMOS and CMOS-on-insulator technologies, with little or no penalty for modified contact and via layout.

Using large-area polysilicon capacitors and 101-stage metal-1 delay-lines in the GEM WAT keys as test vehicles, experiments with split lot reliability screening and life test were performed, first with 240Å gate oxide and then again with 150 Å gate oxide, having demonstrated the effectiveness of in-process screening using the sacrificial metal pattern technique, which results in practically complete elimination of the defective population for the large-area test capacitors and about a factor of two reduction in circuit functionality failures for the delay-line circuits. The finding that in both test lots not all of the delay-line circuit defective populations are eliminated strongly indicates the existence of other factors that are not addressed by gate oxide screening. The extra cost of the method is the added process steps in the deposition and patterning of the sacrificial metal layer and its removal by wet-etching after voltage screening. Experimental results of the two test lots, however, show that there is little or no degradation in circuit performance; namely, there does not appear to be any penalty in metal-polysilicon contact resistance due to wet-etching of the sacrificial metallization followed by re-metallization and alloying, and that there is no difference, within statistical error, in the delay-line circuit yield with the extra processing steps for the sacrificial metallization.

These results show that use of the sacrificial metal pattern for in-process oxide screening is a promising technique in high-density ICs. Further study, with larger number of samples for better statistics, to investigate the effects of voltage-accelerated screening and testing on more complex test

circuits involving finer geometries and double-level metallization is recommended before practical implementation.

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Appendix A

Listing of titles on "oxide breakdown" and "oxide reliability" from a computer search.

```
  1  CR=MCPHERSON JW, P1, 1985 P INT REL PHYS
  1  CR=MCPHERSON JW, 1985, P1, INT REL PHYS S
  1  CR=MCPHERSON JW, 1985, P1, MAR P REL PHYS
  2  CR=MCPHERSON JW, 1985, P1, P INT REL PHYSICS S
  4  CR=MCPHERSON JW, 1985, P1, P INT RELIABILITY PH
  1  CR=MCPHERSON JW, 1985, P1, 23ND P INT REL PHYS
  2  CR=MCPHERSON JW, 1985, P1, 23RD ANN P IEEE INT
  1  CR=MCPHERSON JW, 1985, P1, 23RD ANN P REL PHYS
  1  CR=MCPHERSON JW, 1985, P1, 23RD P IEEE IRPS
  1  CR=MCPHERSON JW, 1985, P1, 23RD P INT REL PHYS
  2  CR=MCPHERSON JW, 1985, P1, 23RD P REL PHYS S
 16  TOTAL (THIS IMPLIES THAT ONE AUTHOR CITED
        THIS PAPER TWICE IN THE SAME ARTICLE
        BECAUSE THE TOTAL SHOULD BE 17)

 3/3/1     (Item 1 from file: 34)
10447027   Genuine Article#: ED146   Number of References: 163
  THE PHYSICS OF SIO2 LAYERS
  VERWEY JF; AMERASEKERA EA; BISSCHOP J
    PHILIPS RES LABS/5600 JA EINDHOVEN//NETHERLANDS/
  REPORTS ON PROGRESS IN PHYSICS, 1990, V53, N10, P1297-1331
  Language: ENGLISH         Document Type: REVIEW

 3/3/2     (Item 2 from file: 34)
10325960   Genuine Article#: DT590   Number of References: 29
  ESTIMATION OF THIN-OXIDE RELIABILITY USING PROPORTIONAL HAZARDS MODELS
  ELSAYED EA; CHAN CK
    RUTGERS STATE UNIV,DEPT IND ENGN/PISCATAWAY//NJ/08855; AT&T BELL
    LABS/WHIPPANY//NJ/07981
  IEEE TRANSACTIONS ON RELIABILITY, 1990, V39, N3, P329-335
  Language: ENGLISH         Document Type: ARTICLE

 3/3/3     (Item 3 from file: 34)
10219821   Genuine Article#: DK332   Number of References: 23
  PROJECTING GATE OXIDE RELIABILITY AND OPTIMIZING RELIABILITY SCREENS
  MOAZZAMI R; HU CM
    UNIV CALIF BERKELEY,DEPT ELECT & COMP SCI/BERKELEY//CA/94720
  IEEE TRANSACTIONS ON ELECTRON DEVICES, 1990, V37, N7, P1643-1650
  Language: ENGLISH         Document Type: ARTICLE

 3/3/4     (Item 4 from file: 34)
10181690   Genuine Article#: DF067   Number of References: 18
  A PROPORTIONAL HAZARDS APPROACH TO CORRELATE SIO2-BREAKDOWN VOLTAGE AND
TIME DISTRIBUTIONS
  CHAN CK
    AT&T BELL LABS,TECH STAFF/WHIPPANY//NJ/07981
  IEEE TRANSACTIONS ON RELIABILITY, 1990, V39, N2, P147-150
  Language: ENGLISH         Document Type: ARTICLE

 3/3/5     (Item 1 from file: 434)
09788005   Genuine Article#: AW890   Number of References: 13
  TEMPERATURE ACCELERATION OF TIME-DEPENDENT DIELECTRIC-BREAKDOWN
  MOAZZAMI R; LEE JC; HU CM
    UNIV CALIF BERKELEY,DEPT ELECT ENGN & COMP SCI/BERKELEY//CA/94720
  IEEE TRANSACTIONS ON ELECTRON DEVICES, 1989, V36, N11, P2462-2465
  Language: ENGLISH         Document Type: ARTICLE
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3/3/6 (Item 2 from file: 434)
09663997 Genuine Article#: AL129 Number of References: 24
MOSFET SCALING LIMITS DETERMINED BY SUBTHRESHOLD CONDUCTION
PIMBLEY JM; MEINDL JD
RENSSELAER POLYTECH INST,DEPT MATH SCI/TROY//NY/12180; RENSSELAER POLYTECH INST,DEPT ELECT COMP & SYSTENGN/TROY//NY/12180
IEEE TRANSACTIONS ON ELECTRON DEVICES, 1989, V36, N9, P1711-1721
Language: ENGLISH Document Type: ARTICLE

3/3/7 (Item 3 from file: 434)
09434652 Genuine Article#: U2075 Number of References: 20
LIFETIME OF THIN OXIDE AND OXIDE-NITRIDE-OXIDE DIELECTRICS WITHIN TRENCH CAPACITORS FOR DRAMS
HIERGEIST P; SPITZER A; ROHL S
SIEMENS AG,CORP RES & DEV,OTTO HAHN RING 6/D-8000 MUNICH 83//FED REP GER/
IEEE TRANSACTIONS ON ELECTRON DEVICES, 1989, V36, N5, P913-919
Language: ENGLISH Document Type: ARTICLE

3/3/8 (Item 4 from file: 434)
09158776 Genuine Article#: R0263 Number of References: 36
MODELING AND CHARACTERIZATION OF GATE OXIDE RELIABILITY
LEE JC; CHEN IC; HU CM
UNIV CALIF BERKELEY,DEPT ELECT ENGN & COMP SCI/BERKELEY//CA/94720
IEEE TRANSACTIONS ON ELECTRON DEVICES, 1988, V35, N12, P2268-2278
Language: ENGLISH Document Type: ARTICLE

3/3/9 (Item 5 from file: 434)
09092075 Genuine Article#: Q4919 Number of References: 100
IN-PROCESS VOLTAGE STRESSING TO INCREASE RELIABILITY OF MOS INTEGRATED-CIRCUITS
SCHNABLE GL; SWARTZ GA
DAVID SARNOFF RES CTR,SUBSIDIARY SRI INT,CN 5300/PRINCETON//NJ/08543
MICROELECTRONICS AND RELIABILITY, 1988, V28, N5, P757-781
Language: ENGLISH Document Type: REVIEW, BIBLIOGRAPHY

3/3/10 (Item 6 from file: 434)
08274386 Genuine Article#: J6534 Number of References: 15
OPERATION, PERFORMANCE, AND RELIABILITY TESTING OF CHARGE-COUPLED-DEVICES FOR STAR TRACKERS
HOPKINSON GR; COCKSHOTT RA; PURLL DJ; SKIPPER MD; TAYLOR B
SIRA LTD,S HILL/CHISLEHURST BR7 5EH/KENT/ENGLAND/; UNIV DURHAM/DURHAM DH1 3HP//ENGLAND/; UNIV LEICESTER/LEICESTER LE1 7RH//ENGLAND/
OPTICAL ENGINEERING, 1987, V26, N8, P725-733
Language: ENGLISH Document Type: ARTICLE

3/3/11 (Item 7 from file: 434)
08167989 Genuine Article#: H8584 Number of References: 47
THE DIELECTRIC RELIABILITY OF INTRINSIC THIN SIO2-FILMS THERMALLY GROWN ON A HEAVILY DOPED SI SUBSTRATE - CHARACTERIZATION AND MODELING
CHEN CF; WU CY; LEE MK; CHEN CN
NATL CHIAO TUNG UNIV,COLL ENGN,INST ELECTR/HSINCHU//TAIWAN/; ELECTR RES & SERV ORG,IND TECHNOL RES INST/HSINCHU//TAIWAN/
IEEE TRANSACTIONS ON ELECTRON DEVICES, 1987, V34, N7, P1540-1552
Language: ENGLISH Document Type: ARTICLE

3/3/12 (Item 8 from file: 434)

07983205 Genuine Article#: G6094 Number of References: 13
ACCELERATED TESTING OF TIME-DEPENDENT BREAKDOWN OF SIO2
CHEN IC; HU CM
UNIV CALIF BERKELEY,DEPT ELECT ENGN & COMP SCI/BERKELEY//CA/94720
IEEE ELECTRON DEVICE LETTERS, 1987, V8, N4, P140-142
Language: ENGLISH Document Type: ARTICLE

3/3/13 (Item 9 from file: 434)
07835690 Genuine Article#: F5892 Number of References: 154
TRENDS IN ADVANCED PROCESS TECHNOLOGY - SUBMICROMETER CMOS DEVICE DESIGN AND PROCESS REQUIREMENTS
BROWN DM; GHEZZO M; PIMBLEY JM
GE,CORP RES & DEV/SCHENECTADY//NY/12301
PROCEEDINGS OF THE IEEE, 1986, V74, N12, P1678-1702
Language: ENGLISH Document Type: REVIEW, BIBLIOGRAPHY

3/3/14 (Item 1 from file: 433)
07579314 Genuine Article#: E3510 Number of References: 4
GATE OXIDE INTEGRITY OF NMOS TRANSISTOR ARRAYS
SWARTZ GA
RCA LABS/PRINCETON//NJ/08540
IEEE TRANSACTIONS ON ELECTRON DEVICES, 1986, V33, N11, P1826-1829
Language: ENGLISH Document Type: NOTE

3/3/15 (Item 2 from file: 433)
07497817 Genuine Article#: D8336 Number of References: 34
TEST CONSIDERATIONS FOR GATE OXIDE SHORTS IN CMOS ICS
SODEN JM; HAWKINS CF
SANDIA NATL LABS,CTR RADIAT HARDENED MICROELECTR,TECH STAFF,DIV 2142/ALBUQUERQUE//NM/87185; UNIV NEW MEXICO,DEPT ELECT & COMP ENGN/ALBUQUERQUE//NM/87131
IEEE DESIGN & TEST OF COMPUTERS, 1986, V3, N4, P56-64
Language: ENGLISH Document Type: ARTICLE

3/3/16 (Item 3 from file: 433)
07463621 Genuine Article#: D5615 Number of References: 57
RELIABILITY CHARACTERIZATION OF A 3-MU-M CMOS/SOS PROCESS
DUGAN MP
RCA CORP,CTR MICROELECTR,DEPT QUAL & RELIABIL ASSURANCE/SOMERVILLE//NJ/08876
RCA REVIEW, 1986, V47, N2, P138-153
Language: ENGLISH Document Type: ARTICLE

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     $0.16  Estimated cost this search
     $0.16  Estimated total session cost   0.004 Hrs.

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 *****           are also now available        *****

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           11057  BREAKDOWN
           33329  RELIABILITY  (January 1969)
     S1      140  OXIDE(W)(BREAKDOWN OR RELIABILITY)
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 1/TI/1
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 1/TI/2
  Title:  A  new  planarization  technique,  using a combination of RIE and
chemical mechanical polish (CMP)
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1/TI/3
Title: The physics of SiO/sub 2/ layers

1/TI/4
Title: Impact of snapback-induced hole injection on gate oxide reliability of N-MOSFETs

1/TI/5
Title: Estimation of thin-oxide reliability using proportional hazards models

1/TI/6
Title: Investigations of oxygen precipitates in Czochralski silicon wafers by using infrared tomography

1/TI/7
Title: Localized corrosion of sputtered aluminum and Al-0.5% Cu alloy thin films in aqueous HF solution. I. Corrosion phenomena

1/TI/8
Title: Projecting gate oxide reliability and optimizing reliability screens

1/TI/9
Title: Gate oxide breakdown by focused ion beam irradiation

1/TI/10
Title: Quest for an NDT method to detect marginal ESD damage to ICs

1/TI/11
Title: Slow transient voltage and ESD breakdown in unprotected MOS gate oxides

1/TI/12
Title: Reliability issues of MOS and bipolar ICs

1/TI/13
Title: Gate oxide breakdown in a SOI CMOS process using mesa isolation

1/TI/14
Title: Gate oxide reliability in a sealed interface local oxidation scheme

1/TI/15
Title: The impact of metal contamination on the quality of thermal SiO/sub 2/
? t 1/3/1-50

1/3/1
03799035 INSPEC Abstract Number: B91002303, C91012609
Title: Circuit reliability simulator-oxide breakdown module
Author(s): Rosenbaum, E.; Lee, P.M.; Moazzami, R.; Ko, P.K.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: International Electron Devices Meeting 1989. Technical Digest (Cat. No.89CH2637-7) p.331-4
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA 913 pp.

U.S. Copyright Clearance Center Code: CH2637-7/89/0000-0331$01.00
Conference Sponsor: IEEE
Conference Date: 3-6 Dec. 1989 Conference Location: Washington, DC, USA

1/3/2
03787402 INSPEC Abstract Number: B91001826
Title: A new_ planarization tY,xweuYV usZwg a ,+O^-ation of RIE and chemical mechanical polish (CMP)
Author(s): Davarik, B.; Koburger, C.W.; Schulz, R.; Warnock, J.D.; Furukawa, T.; Jost, M.; Taur, Y.; Schwittek, W.G.; DeBrosse, J.K.; Kerbaugh, M.L.; Mauer, J.L.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: International Electron Devices Meeting 1989. Technical Digest (Cat. No.89CH2637-7) p.61-4
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA 913 pp.
U.S. Copyright Clearance Center Code: CH2637-7/89/0000-0061$01.00
Conference Sponsor: IEEE
Conference Date: 3-6 Dec. 1989 Conference Location: Washington, DC, USA

1/3/3
03786045 INSPEC Abstract Number: A91012237, B91001820
Title: The physics of SiO/sub 2/ layers
Author(s): Verwey, J.F.; Amerasekera, E.A.; Bisschop, J.
Author Affiliation: Philips Res. Lab., Eindhoven, Netherlands
Journal: Reports on Progress in Physics vol.53, no.10 p.1297-1331
Publication Date: Oct. 1990 Country of Publication: UK
CODEN: RPPHAG ISSN: 0034-4885
U.S. Copyright Clearance Center Code: 0034-4885/90/101297+36$14.00

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03781455 INSPEC Abstract Number: B91002045
Title: Impact of snapback-induced hole injection on gate oxide reliability of N-MOSFETs
Author(s): Mistry, K.R.; Krakauer, D.B.; Doyle, B.S.
Author Affiliation: Digital Equipment Corp., Hudson, MA, USA
Journal: IEEE Electron Device Letters vol.11, no.10 p.460-2
Publication Date: Oct. 1990 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/90/1000-0460$01.00

1/3/5
03758182 INSPEC Abstract Number: B90074614
Title: Estimation of thin-oxide reliability using proportional hazards models
Author(s): Elsayed, E.A.; Chan, C.K.
Author Affiliation: Dept. of Ind. Eng., Rutgers Univ., Piscataway, NJ, USA
Journal: IEEE Transactions on Reliability vol.39, no.3 p.329-35
Publication Date: Aug. 1990 Country of Publication: USA
CODEN: IERQAD ISSN: 0018-9529
U.S. Copyright Clearance Center Code: 0018-9529/90/0800-0329$01.00

1/3/6

03747485 INSPEC Abstract Number: A90147053
Title: Investigations of oxygen precipitates in Czochralski silicon wafers by using infrared tomography
Author(s): Fillard, J.P.
Author Affiliation: Lab. LINCS, Univ. des Sci. et Tech. du Languedoc, Montpellier, France
Journal: Journal of Crystal Growth vol.103, no.1-4 p.71-7
Publication Date: June 1990 Country of Publication: Netherlands
CODEN: JCRGAE ISSN: 0022-0248
U.S. Copyright Clearance Center Code: 0022-0248/90/$03.50
Conference Title: 3rd International Symposium on Defect Recognition and Image Processing in III-V Compounds (DRIP-III)
Conference Date: 22-25 Sept. 1989 Conference Location: Tokyo, Japan

1/3/7
03735961 INSPEC Abstract Number: A90141534
Title: Localized corrosion of sputtered aluminum and Al-0.5% Cu alloy thin films in aqueous HF solution. I. Corrosion phenomena
Author(s): Scully, J.R.; Frankenthal, R.P.; Hanson, K.J.; Siconolfi, D.J. ; Sinclair, J.D.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Journal: Journal of the Electrochemical Society vol.137, no.5 p. 1365-73
Publication Date: May 1990 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

1/3/8
03734838 INSPEC Abstract Number: B90069607
Title: Projecting gate oxide reliability and optimizing reliability screens
Author(s): Moazzami, R.; Hu, C.
Author Affiliation: Dept. of Electr. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: IEEE Transactions on Electron Devices vol.37, no.7 p. 1643-50
Publication Date: July 1990 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/90/0700-1643$01.00

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03733108 INSPEC Abstract Number: B90069494
Title: Gate oxide breakdown by focused ion beam irradiation
Author(s): Nakashima, Y.; Morimoto, H.; Yamamoto, H.; Kato, S.; Watakabe, Y.; Yasuoka, A.
Author Affiliation: Mitsubishi Electr. Corp., Itami, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.1263 p.44-52
Publication Date: 1990 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
Conference Title: Electron-Beam, X-Ray and Ion-Beam Technology: Submicrometer Lithographies IX
Conference Sponsor: SPIE
Conference Date: 7-8 March 1990 Conference Location: San Jose, CA, USA

1/3/10
03720326 INSPEC Abstract Number: B90061795
Title: Quest for an NDT method to detect marginal ESD damage to ICs

Author(s): Yates, R.B.; Edwards, I.M.
Author Affiliation: Sch. of Eng. Inf. Technol., Sheffield City Polytech., UK
Conference Title: IEE Colloquium on 'NDT Evaluation of Electronic Components and Assemblies' (Digest No.094) p.4/1-4
Publisher: IEE, London, UK
Publication Date: 1990 Country of Publication: UK 40 pp.
Conference Sponsor: IEE
Conference Date: 30 May 1990 Conference Location: London, UK

1/3/11
03720226 INSPEC Abstract Number: B90061305
Title: Slow transient voltage and ESD breakdown in unprotected MOS gate oxides
Author(s): Tunnicliffe, M.J.; Dwyer, V.M.; Campbell, D.S.
Author Affiliation: Dept. of Electron. & Electr. Eng., Loughborough Univ. of Technol., UK
Conference Title: Components Engineering, Reliability and Test Conference. CERT '90 p.78-87
Publisher: Electron. Components Inst, Crowborough, UK
Publication Date: 1990 Country of Publication: UK vii+246 pp.
Conference Sponsor: Electron. Components Inst
Conference Date: 9-11 May 1990 Conference Location: Gatwick Airport, UK

1/3/12
03719516 INSPEC Abstract Number: B90061855, C90059779
Title: Reliability issues of MOS and bipolar ICs
Author(s): Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: Proceedings. 1989 IEEE International Conference on Computer Design: VLSI in Computers and Processors (Cat. No.89CH2794-6) p.438-42
Publisher: IEEE Comput. Soc. Press, Washington, DC, USA
Publication Date: 1989 Country of Publication: USA xvii+587 pp.
ISBN: 0 8186 1971 6
U.S. Copyright Clearance Center Code: CH2794-6/89/0000-0438$01.00
Conference Sponsor: IEEE
Conference Date: 2-4 Oct. 1989 Conference Location: Cambridge, MA, USA

1/3/13
03696230 INSPEC Abstract Number: B90055684
Title: Gate oxide breakdown in a SOI CMOS process using mesa isolation
Author(s): Haond, M.; Le Neel, O.; Mascarin, G.; Gonchond, J.P.
Author Affiliation: CNET, Meylan, France
Conference Title: ESSDERC '89. 19th European Solid State Devices Research Conference p.893-6
Editor(s): Heuberger, A.; Ryssel, H.; Lange, P.
Publisher: Springer-Verlag, Berlin, West Germany
Publication Date: 1989 Country of Publication: West Germany xxv+963 pp.
ISBN: 3 540 51000 1
Conference Date: 11-14 Sept. 1989 Conference Location: Berlin, West Germany

1/3/14

03696218 INSPEC Abstract Number: B90055331
Title: Gate oxide reliability in a sealed interface local oxidation scheme
Author(s): Voors, I.J.; Osinski, K.; Vollebregt, F.H.A.; Seams, C.A.
Author Affiliation: Philips Res. Lab., Eindhoven, Netherlands
Conference Title: ESSDERC '89. 19th European Solid State Devices Research Conference p.361-5
Editor(s): Heuberger, A.; Ryssel, H.; Lange, P.
Publisher: Springer-Verlag, Berlin, West Germany
Publication Date: 1989 Country of Publication: West Germany xxv-963 pp.
ISBN: 3 540 51000 1
Conference Date: 11-14 Sept. 1989 Conference Location: Berlin, West Germany

1/3/15
03696209 INSPEC Abstract Number: B90055326
Title: The impact of metal contamination on the quality of thermal SiO/sub 2/
Author(s): Wendt, H.; Cerva, H.
Author Affiliation: Siemens AG, Munchen, West Germany
Conference Title: ESSDERC '89. 19th European Solid State Devices Research Conference p.306-9
Editor(s): Heuberger, A.; Ryssel, H.; Lange, P.
Publisher: Springer-Verlag, Berlin, West Germany
Publication Date: 1989 Country of Publication: West Germany xxv-963 pp.
ISBN: 3 540 51000 1
Conference Date: 11-14 Sept. 1989 Conference Location: Berlin, West Germany

1/3/16
03691848 INSPEC Abstract Number: B90054624
Title: Tunnel-oxide breakdown characteristics of floating-gate-type EEPROM
Author(s): Sato, K.; Fukuzaki, Y.; Hatakeyama, S.; Ikeda, N.
Author Affiliation: Kyoto Res. Lab., Matsushita Electron. Corp., Kyoto, Japan
Journal: Electronics and Communications in Japan, Part 2 (Electronics) vol.72, no.10 p.1-8
Publication Date: Oct. 1989 Country of Publication: USA
CODEN: ECJEEJ ISSN: 8756-663X
U.S. Copyright Clearance Center Code: 8756-663X/89/0009-0001$7.50/0

1/3/17
03678049 INSPEC Abstract Number: B90050199
Title: Impact of oxide thinning at the LOCOS edge of MOS capacitors on constant current stress
Author(s): Kerber, M.; Zeller, Ch.
Author Affiliation: Siemens AG, Munich, West Germany
Conference Title: ESSDERC '89. 19th European Solid State Devices Research Conference p.139-42
Editor(s): Heuberger, A.; Ryssel, H.; Lange, P.
Publisher: Springer-Verlag, Berlin, West Germany
Publication Date: 1989 Country of Publication: West Germany xxv-963 pp.
ISBN: 3 540 51000 1
Conference Date: 11-14 Sept. 1989 Conference Location: Berlin, West Germany

1/3/18
03677950 INSPEC Abstract Number: B90049754
Title: Degradation of gate oxide breakdown characteristics by electrostatic and radiation damage during plasma processing
Author(s): Wu, I.-W.; Bruce, R.H.; Koyanagi, M.; Huang, T.Y.
Author Affiliation: Xerox Palo Alto Res. Center, CA, USA
Conference Title: 1989 International Symposium on VLSI Technology, Systems and Applications. Proceedings of Technical Papers (Cat. No.89CH2631-0) p.222-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA x+393 pp.
Conference Sponsor: IEEE; Nat. Sci. Council; Ind. Technol. Res. Inst
Conference Date: 17-19 May 1989 Conference Location: Taipei, Taiwan

1/3/19
03677286 INSPEC Abstract Number: B90050156
Title: CMOS devices fabricated in thin epitaxial silicon on oxide
Author(s): Leung, D.L.; Cole, R.C.; Cobert, D.M.; Knudsen, J.F.; Hurrell, J.P.; Mayer, D.C.; Newman, R.
Author Affiliation: Aerosp. Corp., El Segundo, CA, USA
Conference Title: 1989 IEEE SOS/SOI Technology Conference (Cat. No.89CH2796-1) p.74-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA v+178 pp.
Conference Sponsor: IEEE
Conference Date: 3-5 Oct. 1989 Conference Location: Stateline, NV, USA

1/3/20
03677283 INSPEC Abstract Number: B90050154
Title: Gate oxide breakdown behaviour in a mesa SOI CMOS process
Author(s): Haond, M.; Le Neel, O.; Mascarin, G.; Gonchond, J.P.
Author Affiliation: CNET, Meylan, France
Conference Title: 1989 IEEE SOS/SOI Technology Conference (Cat. No.89CH2796-1) p.68-9
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA v+178 pp.
Conference Sponsor: IEEE
Conference Date: 3-5 Oct. 1989 Conference Location: Stateline, NV, USA

1/3/21
03660741 INSPEC Abstract Number: B90043774
Title: Defect control in silicon crystals
Author(s): Matsushita, Y.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: 1989 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.89CH2694-8) p.5-8
Publisher: Business Center for Acad. Soc. Japan, Tokyo, Japan
Publication Date: 1989 Country of Publication: Japan xiii+107 pp.
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 22-25 May 1989 Conference Location: Kyoto, Japan

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03608387 INSPEC Abstract Number: B90028282
Title: In-situ processing using rapid thermal chemical vapor deposition
Author(s): Murali, V.; Wu, A.T.; Dass, L.; Frost, M.R.; Fraser, D.B.; Liao, J.; Crowley, J.

Author Affiliation: Intel Corp., Santa Clara, CA, USA
Journal: Journal of Electronic Materials vol.18, no.6 p.731-6
Publication Date: Nov. 1989 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
U.S. Copyright Clearance Center Code: 0361-5235/89/1401-731$05.00

1/3/23
03607480 INSPEC Abstract Number: A90062514, B90028354
Title: Charge trapping in dielectrics grown on polycrystalline silicon
Author(s): Liang, M.-S.; Radjy, N.; Cox, W.; Cagnina, S.
Author Affiliation: Adv. Micro Devices, Sunnyvale, CA, USA
Journal: Journal of the Electrochemical Society vol.136, no.12 p. 3786-90
Publication Date: Dec. 1989 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

1/3/24
03585162 INSPEC Abstract Number: B90022124
Title: Defect-related gate oxide breakdown
Author(s): Bergholz, W.; Mohr, W.; Drewes, W.; Wendt, H.
Author Affiliation: Siemens AG, Semiconductor Div., Munich, West Germany

Journal: Materials Science & Engineering B (Solid-State Materials for Advanced Technology) vol.B4, no.1-4 p.359-66
Publication Date: Oct. 1989 Country of Publication: Switzerland
ISSN: 0921-5107
U.S. Copyright Clearance Center Code: 0921-5107/89/$3.50
Conference Title: Symposium B on Science and Technology of Defects in Silicon of the E-MRS Meeting
Conference Date: 30 May-2 June 1989 Conference Location: Strasbourg, France

1/3/25
03584981 INSPEC Abstract Number: B90022125
Title: Gate oxide breakdown statistics in wearout tests of metal-oxide-semiconductor structures
Author(s): Sune, J.; Placencia, I.; Farres, E.; Barniol, N.; Martin, F.; Aymerich, X.
Author Affiliation: Dept. de Fisica, Univ. Autonoma de Barcelona, Spain
Journal: Microelectronics Journal vol.20, no.6 p.27-39
Publication Date: Nov.-Dec. 1989 Country of Publication: UK
CODEN: MICEB9 ISSN: 0026-2692

1/3/26
03584980 INSPEC Abstract Number: B90022102
Title: Investigation of gate oxide breakdown in CMOS integrated circuits
Author(s): Pesic, B.; Dimitrijev, S.; Stojadinovic, N.
Author Affiliation: Fac. of Electron. Eng., Nis Univ., Yugoslavia
Journal: Microelectronics Journal vol.20, no.6 p.19-26
Publication Date: Nov.-Dec. 1989 Country of Publication: UK
CODEN: MICEB9 ISSN: 0026-2692

1/3/27
03582966 INSPEC Abstract Number: A90040923, B90021609
Title: The effect of aluminum gate thickness on charge trapping in metal-oxide-semiconductor devices
Author(s): Berger, M.; Avni, E.; Shappir, J.

Author Affiliation: Sch. of Appl. Sci. & Technol., Hebrew Univ. of Jerusalem, Israel
Journal: Journal of Applied Physics vol.66, no.10 p.4821-6
Publication Date: 15 Nov. 1989 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
U.S. Copyright Clearance Center Code: 0021-8979/89/224821-06$02.40

1/3/28
03573045 INSPEC Abstract Number: A90041471
Title: Effect of oxidation-induced stacking faults on dielectric breakdown characteristics of thermal silicon dioxide
Author(s): Shirai, H.; Kanaya, K.; Yamaguchi, A.; Shimura, F.
Author Affiliation: Huels Japan Ltd., Utsunomiya, Japan
Journal: Journal of Applied Physics vol.66, no.11 p.5651-3
Publication Date: 1 Dec. 1989 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
U.S. Copyright Clearance Center Code: 0021-8979/89/235651-03$02.40

1/3/29
03571827 INSPEC Abstract Number: A90042218
Title: A method for high sensitivity deuterium measurements by means of the D(/sup 3/He,p)/sup 4/He reaction and its applications
Author(s): Qi Oiu; Arai, E.; Aratani, M.; Yanokura, M.; Nozaki, T.; Ohji, Y.; Imura, R.
Author Affiliation: Tokyo Inst. of Technol., Japan
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) vol.B44, no.2 p.179-83
Publication Date: Dec. 1989 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
U.S. Copyright Clearance Center Code: 0168-583X/89/$03.50

1/3/30
03569055 INSPEC Abstract Number: A90028626, B90014909
Title: Gate oxide breakdown statistics in constant-current stressed MOS devices
Author(s): Sune, J.; Placencia, I.; Farres, E.; Barniol, N.; Aymerich, X.
Author Affiliation: Dept. de Fisica, Univ. Autonoma de Barcelona, Spain
Conference Title: 17th Yugoslav Conference on Microelectronics. Proceedings p.839-44 vol.2
Publisher: Elsevier Adv. Technol, Oxford, UK
Publication Date: 1989 Country of Publication: UK 2 vol. 982 pp.
ISBN: 0 948577 33 9
Conference Sponsor: Electron. Ind. Nis; Federal Assoc. Republic Sci. Councils; et al
Conference Date: 9-11 May 1989 Conference Location: Nis, Yugoslavia

1/3/31
03569013 INSPEC Abstract Number: B90015191
Title: Oxide reliability in tungsten polycide gate electrode
Author(s): Kurachi, I.; Yanai, T.; Yoshioka, K.
Author Affiliation: Oki Electr. Ind. Co. Ltd., Tokyo, Japan
Conference Title: 1989 Proceedings. Sixth International IEEE VLSI Multilevel Interconnection Conference (Cat. No.89TH0259-2) p.505
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA 508 pp.
U.S. Copyright Clearance Center Code: TH-0259-2/89/0000-0505$01.00
Conference Sponsor: IEEE

Conference Date: 12-13 June 1989 Conference Location: Santa Clara, CA, USA

1/3/32
03524757 INSPEC Abstract Number: B90001618
Title: A new insight into the p-n junction characteristics of ULSI-the time dependent junction breakdown (TDJB)
Author(s): Matsuoka, H.; Hisamoto, D.; Izawa, R.; Takeda, E.
Author Affiliation: Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Conference Title: Extended Abstracts of the 21st Conference on Solid State Devices and Materials p.129-32
Publisher: Bus. Center for Acad. Soc. Japan, Tokyo, Japan
Publication Date: 1989 Country of Publication: Japan viii+604 pp.
ISBN: 4 930813 35 2
Conference Sponsor: Japan Soc. Appl. Phys
Conference Date: 28-30 Aug. 1989 Conference Location: Tokyo, Japan

1/3/33
03505591 INSPEC Abstract Number: B89075986
Title: Novel test structure to study location of breakdown for trench capacitor
Author(s): Kishi, K.; Yoshida, T.; Watanabe, T.; Tanaka, T.; Shinozaki, S.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: ICMTS 1989. Proceedings of the 1989 International Conference on Microelectronic Test Structures (Cat. No.89CH2693-0) p. 245-50
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA xii+265 pp.
ISBN: 0 87942 714 0
U.S. Copyright Clearance Center Code: CH2693-0/89/0000-245$01.00
Conference Sponsor: IEEE; IEE
Conference Date: 13-14 March 1989 Conference Location: Edinburgh, UK

1/3/34
03505565 INSPEC Abstract Number: B89075757
Title: Evaluation technique of gate oxide reliability with electrical and optical measurements
Author(s): Uraoka, Y.; Tsutsu, N.; Morii, T.; Nakata, Y.; Esaki, H.
Author Affiliation: Matsushita Electr. Ind. Co., Ltd., Osaka, Japan
Conference Title: ICMTS 1989. Proceedings of the 1989 International Conference on Microelectronic Test Structures (Cat. No.89CH2693-0) p. 97-102
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA xii+265 pp.
ISBN: 0 87942 714 0
U.S. Copyright Clearance Center Code: CH2693-0/89/0000-097$01.00
Conference Sponsor: IEEE; IEE
Conference Date: 13-14 March 1989 Conference Location: Edinburgh, UK

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03500747 INSPEC Abstract Number: A89137476, B89075737
Title: Electrical evaluation of wet and dry cleaning procedures for silicon device fabrication
Author(s): Ruzyllo, J.; Hoff, A.M.; Frystak, D.C.; Hossain, S.D.
Author Affiliation: Dept. of Electr. Eng., Pennsylvania State Univ., University Park, PA, USA

Journal: Journal of the Electrochemical Society vol.136, no.5 p. 1474-6
Publication Date: May 1989 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

1/3/36
03499819 INSPEC Abstract Number: B89075726
Title: A study of contamination and damage on Si surfaces induced by dry etching
Author(s): Moghadam, F.K.; Mu, X.-C.
Author Affiliation: Intel Corp., Santa Clara, CA, USA
Journal: IEEE Transactions on Electron Devices vol.36, no.9, pt.1 p.1602-9
Publication Date: Sept. 1989 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/89/0900-1602$01.00

1/3/37
03477980 INSPEC Abstract Number: B89069203
Title: Breakdown yield and lifetime of thin gate oxides in CMOS processing
Author(s): Wu, I.-W.; Koyanagi, M.; Holland, S.; Huang, T.Y.; Mikkelsen, J.C., Jr.; Bruce, R.H.; Chiang, A.
Author Affiliation: Xerox Palo Alto Res. Center, Electron. & Imaging Lab., CA, USA
Journal: Journal of the Electrochemical Society vol.136, no.6 p. 1638-45
Publication Date: June 1989 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

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03462530 INSPEC Abstract Number: B89061412
Title: Extensions of the effective thickness theory of oxide breakdown
Author(s): Coleman, D.J., Jr.; Hunter, W.R.; Brown, G.A.; Chen, I.-C.
Author Affiliation: Texas Instrum., Dallas, TX, USA
Conference Title: 27th Annual Proceedings. Reliability Physics 1989 (Cat. No.89CH2650-0) p.39-42
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA 259 pp.
U.S. Copyright Clearance Center Code: CH2650-0/89/0000-0039$01.00
Conference Sponsor: IEEE
Conference Date: 11-13 April 1989 Conference Location: Phoenix, AZ, USA

1/3/39
03462526 INSPEC Abstract Number: B89061408
Title: Interface degradation and dielectric breakdown of thin oxides due to homogeneous charge injection
Author(s): Kerber, M.; Schwalke, U.
Author Affiliation: Siemens AG, Munich, West Germany
Conference Title: 27th Annual Proceedings. Reliability Physics 1989 (Cat. No.89CH2650-0) p.17-21
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA 259 pp.
U.S. Copyright Clearance Center Code: CH2650-0/89/0000-0017$01.00
Conference Sponsor: IEEE
Conference Date: 11-13 April 1989 Conference Location: Phoenix, AZ, USA

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03432122 INSPEC Abstract Number: B89054985
Title: Influence of structure process flow and high current implantation on gate oxide degradation
Author(s): Ploss, R.; Harley-Stead, M.; Weisshuhn, S.; Lehner, K.; Glawischnig, H.
Author Affiliation: Siemens, Munchen, West Germany
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) vol.B36, no.4 p.439-45
Publication Date: April 1989 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
U.S. Copyright Clearance Center Code: 0168-583X/89/$03.50

1/3/41
03416393 INSPEC Abstract Number: B89048659
Title: Radiation hardened VHSIC CMOS/SOS process
Author(s): Chung, L.; Tocci, L.; Liu, P.; Fraser, J.; White, J.; Colesworthy, R.; Brandewie, J.; Kjar, R.
Conference Title: 1988 IEEE SOS/SOI Technology Workshop. Proceedings (IEEE Cat. No.88CH2698-9) p.82
Publisher: IEEE, New York, NY, USA
Publication Date: 1988 Country of Publication: USA 82 pp.
Conference Sponsor: IEEE
Conference Date: 3-5 Oct. 1988 Conference Location: St. Simons Island, GA, USA

1/3/42
03398694 INSPEC Abstract Number: B89042923
Title: Submicron bipolar-CMOS technology using 16 GHz f/sub T/ double poly-Si bipolar devices
Author(s): Yuzuriha, T.; Yamaguchi, T.; Lee, J.
Author Affiliation: Tektronix Inc., Beaverton, OR, USA
Conference Title: International Electron Devices Meeting. Technical Digest (IEEE Cat. No.88CH2528-8) p.748-51
Publisher: IEEE, New York, NY, USA
Publication Date: 1988 Country of Publication: USA 902 pp.
U.S. Copyright Clearance Center Code: CH2528-8/88/0000-0748$01.00
Conference Sponsor: IEEE
Conference Date: 11-14 Dec. 1988 Conference Location: San Francisco, CA, USA

1/3/43
03394573 INSPEC Abstract Number: B89042655
Title: Thin dielectric quality/yield study using a constant voltage ramp method
Author(s): Bryant, F.; Fu-Tai Liou; Yu-Pin Han; Barnes, J.J.
Author Affiliation: SGS-Thomson Microelectron., Carrollton, TX, USA
Journal: Journal of the Electrochemical Society vol.136, no.1 p. 283-7
Publication Date: Jan. 1989 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

1/3/44
03380312 INSPEC Abstract Number: B89036987
Title: Stress induced leakage current limiting to scale down EEPROM tunnel oxide thickness

Author(s): Naruke, K.; Taguchi, S.; Wada, M.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: International Electron Devices Meeting. Technical Digest (IEEE Cat. No.88CH2528-8) p.424-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1988 Country of Publication: USA 902 pp.
U.S. Copyright Clearance Center Code: CH2528-8/88/0000-0424$01.00
Conference Sponsor: IEEE
Conference Date: 11-14 Dec. 1988 Conference Location: San Francisco, CA, USA

1/3/45
03334487 INSPEC Abstract Number: B89022733
Title: The tunnel-oxide breakdown characteristics of floating-gate-type EEPROM
Author(s): Sato, K.; Fukuzaki, Y.; Hatakeyama, S.; Ikeda, N.
Author Affiliation: Kyoto Res. Lab., Matsushita Electron. Corp., Japan
Journal: Transactions of the Institute of Electronics, Information and Communication Engineers C vol.J71C, no.11 p.1529-35
Publication Date: Nov. 1988 Country of Publication: Japan
CODEN: DJTCEX ISSN: 0913-5723

1/3/46
03331998 INSPEC Abstract Number: B89023484
Title: Modeling and characterization of gate oxide reliability
Author(s): Lee, J.C.; Chen Ih-Chin; Hu Chenming
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: IEEE Transactions on Electron Devices vol.35, no.12 p. 2268-78
Publication Date: Dec. 1988 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/88/1200-2268$01.00

1/3/47
03331996 INSPEC Abstract Number: B89023820
Title: The effect of channel hot-carrier stressing on gate-oxide integrity in MOSFETs
Author(s): Chen Ih-Chin; Choi Jeong Yeol; Hu Chenming
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: IEEE Transactions on Electron Devices vol.35, no.12 p. 2253-8
Publication Date: Dec. 1988 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/88/1200-2253$01.00

1/3/48
03319806 INSPEC Abstract Number: B89014785
Title: Design considerations for the operation of CMOS inverters at cryogenic temperatures
Author(s): Deen, M.J.; Jing Wang
Author Affiliation: Sch. of Eng. Sci., Simon Fraser Univ., Burnaby, BC, Canada
Conference Title: Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors p.108-16
Editor(s): Raider, S.I.; Kirschman, R.; Hayakawa, H.; Ohta, H.

Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1988 Country of Publication: USA xii+602 pp.
Conference Date: 19-23 Oct. 1987 Conference Location: Honolulu, HI, USA

1/3/49
03276987 INSPEC Abstract Number: B89002273
Title: New ESD test method
Author(s): Satoh, Y.; Matsumoto, H.; Shimotori, K.; Ishida, S.
Author Affiliation: Mitsubishi Electric Corp., Hyogo, Japan
Conference Title: Proceedings ISTFA 1986: International Symposium for Testing and Failure Analysis 1986 p.91-4
Publisher: ASM Int, Metals Park, OH, USA
Publication Date: 1986 Country of Publication: USA xiii+327 pp.
ISBN: 0 87170 236 3
Conference Date: 20-24 Oct. 1986 Conference Location: Los Angeles, CA, USA

1/3/50
03259143 INSPEC Abstract Number: B88071373
Title: The new concept of thin oxide breakdown mechanism
Author(s): Tatsuuma, K.; Sugimoto, M.; Ajiki, T.
Author Affiliation: Matsushita Electron. Corp., Kyoto, Japan
Conference Title: 1988 Symposium on VLSI Technology. Digest of Technical Papers p.43-4
Publisher: Japan Soc. Appl. Phys, Tokyo, Japan
Publication Date: 1988 Country of Publication: Japan 104 pp.
Conference Sponsor: Japan Soc. Appl. Phys.; IEEE
Conference Date: 10-13 May 1988 Conference Location: San Diego, CA, USA
? t 1/3/51-100

1/3/51
03259142 INSPEC Abstract Number: B88071372
Title: Oxide breakdown wearout limitation on thermally grown thin gate oxide
Author(s): Hokari, Y.
Author Affiliation: NEC Corp., Kanagawa, Japan
Conference Title: 1988 Symposium on VLSI Technology. Digest of Technical Papers p.41-2
Publisher: Japan Soc. Appl. Phys, Tokyo, Japan
Publication Date: 1988 Country of Publication: Japan 104 pp.
Conference Sponsor: Japan Soc. Appl. Phys.; IEEE
Conference Date: 10-13 May 1988 Conference Location: San Diego, CA, USA

1/3/52
03259140 INSPEC Abstract Number: B88071592
Title: The effect of hydrogen on hot carrier immunity, radiation hardness and gate oxide reliability in MOS devices
Author(s): Nissan-Cohen, Y.; Woodbury, H.H.; Gorczyca, T.B.; Wei, C.-Y.
Author Affiliation: General Electric Corp. Res. & Dev., Schenectady, NY, USA
Conference Title: 1988 Symposium on VLSI Technology. Digest of Technical Papers p.37-8
Publisher: Japan Soc. Appl. Phys, Tokyo, Japan
Publication Date: 1988 Country of Publication: Japan 104 pp.

Conference Sponsor: Japan Soc. Appl. Phys.; IEEE
Conference Date: 10-13 May 1988 Conference Location: San Diego, CA, USA

1/3/53
03223359 INSPEC Abstract Number: A88124892
Title: A model for silicon-oxide breakdown under high field and current stress
Author(s): Avni, E.; Shappir, J.
Author Affiliation: Div. of Appl. Phys., Hebrew Univ. of Jerusalem, Israel
Journal: Journal of Applied Physics vol.64, no.2 p.743-8
Publication Date: 15 July 1988 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
U.S. Copyright Clearance Center Code: 0021-8979/88/140743-06$02.40

1/3/54
03218978 INSPEC Abstract Number: B88057662
Title: The effect of channel hot carrier stressing on gate oxide integrity in MOSFET
Author(s): Chen, I.C.; Choi, J.Y.; Chan, T.Y.; Ong, T.C.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: 26th Annual Proceedings. Reliability Physics 1988 (Cat. No.88CH2508-0) p.1-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1988 Country of Publication: USA x+255 pp.
U.S. Copyright Clearance Center Code: CH2508-0/88/0000-0001$01.00
Conference Sponsor: IEEE
Conference Date: 12-14 April 1988 Conference Location: Monterey, CA, USA

1/3/55
03209238 INSPEC Abstract Number: B88057449
Title: Rapid thermal annealing effects on gate oxide of ion implanted devices
Author(s): Hashemi, F.; Paz de Araujo, C.A.
Author Affiliation: Harris Semicond., Melbourne, FL, USA
Journal: Semiconductor International vol.11, no.6 p.152-7
Publication Date: May 1988 Country of Publication: USA
CODEN: SITLDD ISSN: 0163-3767

1/3/56
03198149 INSPEC Abstract Number: B88051034
Title: Statistical and graphical analyses of oxide thickness and ESD failure modes
Author(s): Satterfield, H.W.; Werber, R.F.
Author Affiliation: Harris Semicond., Melbourne, FL, USA
Conference Title: Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1987 p.258-64
Publisher: EOS/ESD Assoc, Rome, NY, USA
Publication Date: 1987 Country of Publication: USA xiii+318 pp.
Conference Sponsor: EOS/ESD Assoc.; ITT Res. Inst
Conference Date: 29 Sept.-1 Oct. 1987 Conference Location: Orlando, FL, USA

1/3/57

03198148 INSPEC Abstract Number: B88050865
Title: The effects of high electric field transients on thin gate oxide MOSFETs
Author(s): Fong, Y.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1987- p.252-7
Publisher: EOS/ESD Assoc, Rome, NY, USA
Publication Date: 1987 Country of Publication: USA xiii+318 pp.
Conference Sponsor: EOS/ESD Assoc.; ITT Res. Inst
Conference Date: 29 Sept.-1 Oct. 1987 Conference Location: Orlando, FL, USA

1/3/58
03198139 INSPEC Abstract Number: B88051023
Title: Analysis of high-voltage ESD pulse testing on CMOS gate array technology
Author(s): Hull, R.; Jackson, R.
Author Affiliation: United Technols. Microelectron. Center, Colorado Springs, CO, USA
Conference Title: Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1987 p.200-4
Publisher: EOS/ESD Assoc, Rome, NY, USA
Publication Date: 1987 Country of Publication: USA xiii+318 pp.
Conference Sponsor: EOS/ESD Assoc.; ITT Res. Inst
Conference Date: 29 Sept.-1 Oct. 1987 Conference Location: Orlando, FL, USA

1/3/59
03179284 INSPEC Abstract Number: B88044625
Title: Synchrotron section topographic and device yield studies of backside gettered silicon wafers
Author(s): Partanen, J.; Tuomi, T.; Tilli, M.; Hahn, S.; Wong, C.-C.D.
Author Affiliation: Helsinki Univ. of Technol., Espoo, Finland
Conference Title: 2nd International Autumn Meeting Proceedings: Gettering and Defect Engineering in the Semiconductor Technology (GADEST '87) p. 313-17
Editor(s): Richter, H.
Publisher: Akad. Wissenschaften DDR, Frankfurt (Oder), East Germany
Publication Date: 1987 Country of Publication: East Germany viii+367 pp.
Conference Sponsor: Acad. Sci. GDR; VEB Kombinat Mikroelektronik; Phys. Soc. GDR
Conference Date: 11-17 Oct. 1987 Conference Location: Garzau, East Germany

1/3/60
03168641 INSPEC Abstract Number: A88094072
Title: Interaction of a polycrystalline silicon/SiO/sub 2//silicon substrate under thermal/electrical fields
Author(s): Chou, T.C.; Tu, K.N.
Author Affiliation: IBM Res. Div., Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: Applied Physics Letters vol.52, no.16 p.1317-19
Publication Date: 18 April 1988 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951

U.S. Copyright Clearance Center Code: 0003-6951/88/161317-03$01.00

1/3/61
03157396 INSPEC Abstract Number: B88039700
Title: Novel germanium channel-stop implantation for submicron CMOS
Author(s): Pfiester, J.R.; Alvis, J.R.
Author Affiliation: Motorola Inc., Austin, TX, USA
Conference Title: 1987 International Electron Devices Meeting, IEDM. Technical Digeset (Cat. No.87CH2515-5) p.740-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1987 Country of Publication: USA 936 pp.
U.S. Copyright Clearance Center Code: CH2515-5/87/0000-0740$01.00
Conference Sponsor: IEEE
Conference Date: 6-9 Dec. 1987 Conference Location: Washington, DC, USA

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03134017 INSPEC Abstract Number: B88033043
Title: Thin silicon dioxide using the rapid thermal oxidation (RTO) process for trench capacitors
Author(s): Miyai, Y.; Yoneda, K.; Oishi, H.; Uchida, H.; Inoue, M.
Author Affiliation: Matsushita Electron. Corp., Kyoto Res. Lab., Japan
Journal: Journal of the Electrochemical Society vol.135, no.1 p. 150-5
Publication Date: Jan. 1988 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

1/3/63
03133995 INSPEC Abstract Number: B88033041
Title: Oxide breakdown due to charge accumulation during plasma etching
Author(s): Ryden, K.-H.; Norstrom, H.; Nender, C.; Berg, S.
Author Affiliation: Inst. of Microwave Technol., Stockholm, Sweden
Journal: Journal of the Electrochemical Society vol.134, no.12 p. 3113-18
Publication Date: Dec. 1987 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

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03109775 INSPEC Abstract Number: B88026271
Title: Common origin for electron and hole traps in MOS devices
Author(s): Aslam, M.
Author Affiliation: Dept. of Electr. & Comput. Eng., Wayne State Univ., Detroit, MI, USA
Journal: IEEE Transactions on Electron Devices vol.ED-34, no.12, pt.1 p.2535-9
Publication Date: Dec. 1987 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/87/1200-2535$01.00

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03106076 INSPEC Abstract Number: A88056235
Title: Evidence of the role of defects near the injecting interface in determining SiO/sub 2/ breakdown
Author(s): Olivo, P.; Ricco, B.; Nguyen, T.N.; Kuan, T.S.; Jeng, S.J.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: Applied Physics Letters vol.51, no.26 p.2245-7

Publication Date: 28 Dec. 1987 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/87/522245-03$01.00

1/3/66
03106059 INSPEC Abstract Number: A88048896, B88025980
Title: Low-frequency noise in silicon-gate metal-oxide-silicon capacitors before oxide breakdown
Author(s): Neri, B.; Olivo, P.; Ricco, B.
Author Affiliation: Istituto di Elettronica e Telecommun., Pisa Univ., Italy
Journal: Applied Physics Letters vol.51, no.25 p.2167-9
Publication Date: 21 Dec. 1987 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/87/512167-03$01.00

1/3/67
03098710 INSPEC Abstract Number: B88019842
Title: The effect of charge build-up on gate oxide breakdown during dry etching
Author(s): Tsunokuni, K.; Nojiri, K.; Kuboshima, S.; Hirobe, K.
Author Affiliation: Musashi Works, Hitachi, Ltd, Tokyo, Japan
Conference Title: Extended Abstracts of the 19th Conference on Solid State Devices and Materials p.195-8
Publisher: Bus. Center Acad. Soc. Japan, Tokyo, Japan
Publication Date: 1987 Country of Publication: Japan vii+565 pp.
ISBN: 4 930813 21 2
Conference Sponsor: Japan Soc. Appl. Phys.; Inst. Electron. Inf. & Commun. Eng.; IEEE; et al
Conference Date: 25-27 Aug. 1987 Conference Location: Tokyo, Japan

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03095465 INSPEC Abstract Number: B88019833
Title: Recent progress in dry etching technology for advanced VLSI devices
Author(s): Horiike, Y.; Arikado, T.; Horioka, K.; Sekine, M.; Nishino, H.; Hayasaka, N.; Okano, H.
Author Affiliation: VLSI Res. Center, Toshiba Corp., Kawasaki, Japan
Journal: Le Vide les Couches Minces no.237, suppl. p.173-81
Publication Date: 1987 Country of Publication: France
CODEN: VCMIDS ISSN: 0223-4335
Conference Title: CIP G87: 6eme Colloque International sur les Plasmas et la Pulverisation Cathodique et 4eme Symposium International sur la Gravure Seche et le Depot Plasma et Microelectronique (CIP G87: 6th International Colloquium on Plasmas and Cathodic Sputtering and 4th International Symposium on Dry Etching and Plasma Deposition in Microelectronics)
Conference Date: 1-5 June 1987 Conference Location: Antibes, France

1/3/69
03059323 INSPEC Abstract Number: B88007616
Title: Effects of titanium salicide process on oxide charge trapping and hot-electron reliability in submicron MOS devices for VLSI
Author(s): Chang, S.-T.; Chiu, K.
Author Affiliation: Hewlett-Packard Labs., Palo Alto, CA, USA
Conference Title: 1987 Symposium on VLSI Technology. Digest of Technical Papers p.65-6
Publisher: Bus. Center Acad. Soc. Japan, Tokyo, Japan
Publication Date: 1987 Country of Publication: Japan 113 pp.

Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 18-21 May 1987 Conference Location: Karuizawa, Japan

1/3/70
03058408 INSPEC Abstract Number: B88007606
Title: The electrical properties of MOS transistors fabricated with direct ion beam nitridation
Author(s): Han-Sheng Lee
Author Affiliation: Dept. of Electron., General Motors Res. Labs., Warren, MI, USA
Conference Title: Emerging Semiconductor Technology. ASTM Special Technical Publication 960. Fourth International Symposium on Semiconductor Processing p.150-9
Editor(s): Gupta, D.C.; Langer, P.H.
Publisher: ASTM, Philadelphia, PA, USA
Publication Date: 1987 Country of Publication: USA 704 pp.
ISBN: 0 8031 0459 6
Conference Sponsor: ASTM; NBS; IEEE; et al
Conference Date: 28-31 Jan. 198[illegible] Conference Location: San Jose, CA, USA

1/3/71
03054192 INSPEC Abstract Number: A88015207, B88007656
Title: Evaluation of thin oxides grown by the atomic oxygen afterglow method
Author(s): Ruzyllo, J.; Hoff, A.; Ruggles, G.
Author Affiliation: Dept. of Electr. Eng., Pennsylvania State Univ., University Park, PA, USA
Journal: Journal of Electronic Materials vol.16, no.5 p.373-8
Publication Date: Sept. 1987 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
U.S. Copyright Clearance Center Code: 0361-5235/1987/1401-373$5.00

1/3/72
03053088 INSPEC Abstract Number: A88021536, B88007372
Title: The nature of charge trapping responsible for thin-oxide breakdown under a dynamic field stress
Author(s): Haddad, S.; Liang, M.-S.
Author Affiliation: Adv. Micro Devices Inc., Sunnyvale, CA, USA
Journal: IEEE Electron Device Letters vol.EDL-8, no.11 p.524-7
Publication Date: Nov. 1987 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/87/1100-0524$01.00

1/3/73
03038748 INSPEC Abstract Number: B88001465
Title: A new failure mode of very thin (<50 AA) thermal SiO/sub 2/ films
Author(s): Nguyen, T.N.; Olivo, P.; Ricco, B.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: 25th Annual Proceedings: Reliability Physics 1987 (Cat. No.87CH2388-7) p.66-71
Publisher: IEEE, New York, NY, USA
Publication Date: 1987 Country of Publication: USA viii+279 pp.
U.S. Copyright Clearance Center Code: CH2388-7/87/0000-0066$01.00
Conference Sponsor: IEEE
Conference Date: 7-9 April 1987 Conference Location: San Diego, CA,

USA

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03010176 INSPEC Abstract Number: A87138066, B87074118
Title: Gate oxide integrity and minority-carrier lifetime correlated with Si wafer polish damage
Author(s): Lee, J.; Wong, C.-C.D.; Tung, C.Y.; Smith, W.L.; Hahn, S.; Arst, M.
Author Affiliation: Integrated Device Technol., Inc., Santa Clara, CA, USA
Journal: Applied Physics Letters vol.51, no.1 p.54-6
Publication Date: 5 July 1987 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/87/270054-03$01.00

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02956350 INSPEC Abstract Number: B87053568
Title: Degradation of very thin gate oxide MOS devices under dynamic high field/current stress
Author(s): Liang, M.; Haddad, S.; Cox, W.; Cagnina, S.
Author Affiliation: Adv. Micro Devices Inc., Sunnyvale, CA, USA
Conference Title: International Electron Devices Meeting 1986. Technical Digest (Cat. No.86CH2381-2) p.394-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA 834 pp.
U.S. Copyright Clearance Center Code: CH2381-2/86/0000-0394$01.00
Conference Sponsor: IEEE
Conference Date: 7-10 Dec. 1986 Conference Location: Los Angeles, CA, USA

1/3/76
02956347 INSPEC Abstract Number: B87053565
Title: Reliability in submicron MOSFETs stressed at 77 K
Author(s): Toriumi, A.; Iwase, M.; Wada, T.; Taniguchi, K.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: International Electron Devices Meeting 1986. Technical Digest (Cat. No.86CH2381-2) p.382-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA 834 pp.
U.S. Copyright Clearance Center Code: CH2381-2/86/0000-0382$01.00
Conference Sponsor: IEEE
Conference Date: 7-10 Dec. 1986 Conference Location: Los Angeles, CA, USA

1/3/77
02939631 INSPEC Abstract Number: A87099088
Title: Electron-trap generation by recombination of electrons and holes in SiO/sub 2/
Author(s): Chen, I.C.; Holland, S.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: Journal of Applied Physics vol.61, no.9 p.4544-8
Publication Date: 1 May 1987 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
U.S. Copyright Clearance Center Code: 0021-8979/87/094544-05$02.40

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02933418 INSPEC Abstract Number: A87092595, B87045810
Title: Oxide breakdown dependence on thickness and hole current-enhanced reliability of ultra thin oxides
Author(s): Chen, I.C.; Holland, S.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: International Electron Devices Meeting 1986. Technical Digest (Cat. No.86CH2381-2) p.660-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA 834 pp.
U.S. Copyright Clearance Center Code: CH2381-2/86/0000-0660$01.00
Conference Sponsor: IEEE
Conference Date: 7-10 Dec. 1986 Conference Location: Los Angeles, CA, USA

1/3/79
02933359 INSPEC Abstract Number: B87046126
Title: Characterization of IC devices fabricated in low temperature (550 degrees C) epitaxy by UHV/CVD technique
Author(s): Nguyen, T.N.; Harame, D.L.; Stork, J.M.C.; LeGoues, F.K.; Meyerson, B.S.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: International Electron Devices Meeting 1986. Technical Digest (Cat. No.86CH2381-2) p.304-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA 834 pp.
U.S. Copyright Clearance Center Code: CH2381-2/86/0000-0304$01.00
Conference Sponsor: IEEE
Conference Date: 7-10 Dec. 1986 Conference Location: Los Angeles, CA, USA

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02886742 INSPEC Abstract Number: A87064267, B87032438
Title: Correlation of carrier trapping and oxide breakdown with H/sub 2/O partial pressures in pyrogenic oxides
Author(s): Vengurlekar, A.S.; Lakshmanna, V.; Pamanathan, K.V.
Author Affiliation: Tata Inst. of Fundamental Res., Bombay, India
Conference Title: Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials p.467-70
Publisher: Bus. Center Acad. Socs. Japan, Tokyo, Japan
Publication Date: 1986 Country of Publication: Japan x+821 pp.
ISBN: 4 930813 14 X
Conference Sponsor: Japan Soc. Appl. Phys.; IEEE; Electrochem. Soc. Japan ; et al
Conference Date: 20-22 Aug. 1986 Conference Location: Tokyo, Japan

1/3/81
02886649 INSPEC Abstract Number: B87032561
Title: Oxide breakdown in MOS structures under ESD and continuous voltage stress conditions
Author(s): Amerasekera, E.A.; Campbell, D.S.
Author Affiliation: Dept. of Electron. & Electr. Eng., Loughborough Univ. of Technol., UK
Conference Title: Reliability Technology: Theory and Applications. European Reliability Conference - REL-CON '86 p.325-30
Editor(s): Moltoft, J.; Jensen, F.

Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1986 Country of Publication: Netherlands x+461 pp.
ISBN: 0 444 70039 0
Conference Sponsor: Convention Nat. Soc. Electr. Eng. Western Eur.; Danish Soc. Chem., Civil, Electr. & Mech. Eng.; Soc. Eng. Denmark
Conference Date: 16-20 June 1986 Conference Location: Copenhagen, Denmark

1/3/82
02879400 INSPEC Abstract Number: B87032512
Title: Gate-oxide integrity of silicon-on-insulator transistors
Author(s): Kamins, T.I.
Author Affiliation: Hewlett-Packard Labs., Palo Alto, CA, USA
Journal: Electronics Letters vol.23, no.4 p.175-6
Publication Date: 12 Feb. 1987 Country of Publication: UK
CODEN: ELLEAK ISSN: 0013-5194
U.S. Copyright Clearance Center Code: 0013-5194/87/$2.00+0.00

1/3/83
02870074 INSPEC Abstract Number: A87059144
Title: Thickness dependence of oxide breakdown under high field and current stress
Author(s): Liang, M.-S.; Choi, J.Y.
Author Affiliation: Electron. Res. Lab., California Univ., CA, USA
Journal: Applied Physics Letters vol.50, no.2 p.104-6
Publication Date: 12 Jan. 1987 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/87/020104-03$01.00

1/3/84
02844136 INSPEC Abstract Number: A87038217, B87017896
Title: Effectiveness of CVD thin film backside gettering and its interaction with intrinsic gettering
Author(s): Wong, C.-C.D.; Hahn, S.; Ponce, F.A.; Rek, Z.U.
Author Affiliation: IDT Santa Clara, CA, USA
Conference Title: Materials Issues in Silicon Integrated Circuit Processing Symposium p.33-8
Editor(s): Wittmer, M.; Stimmell, J.; Strathman, M.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1986 Country of Publication: USA xvii+535 pp.
ISBN: 0 931837 37 5
Conference Sponsor: Mater. Res. Soc
Conference Date: 15-18 April 1986 Conference Location: Palo Alto, CA, USA

1/3/85
02843638 INSPEC Abstract Number: B87017889
Title: Optimization of etched trench surface for low fixed oxide charges and interface states
Author(s): Chow, P.D.; Jang, C.; Bol, I.; Wang, K.L.
Author Affiliation: Micro-Electron. Center, Xerox Corp., El Segundo, CA, USA
Conference Title: Proceedings of the Fifth International Symposium on Silicon Materials Science and Technology: Semiconductor Silicon 1986 p. 527-35
Editor(s): Huff, H.R.; Abe, T.; Kolbesen, B.

Publisher: Electrochem Soc, Pennington, NJ, USA
Publication Date: 1986 Country of Publication: USA xiv+1096 pp.
Conference Sponsor: Electrochem. Soc
Conference Date: 5-9 May 1986 Conference Location: Boston, MA, USA

1/3/86
02843143 INSPEC Abstract Number: A87039776, B87017977
Title: Anodic oxidation of silicon in pure water
Author(s): Gaspard, F.; Halimaoui, A.
Author Affiliation: Lab. de Spectrometrie Phys., Univ. Sci. et Med. de Grenoble, St. Martin d'Heres, France
Conference Title: Insulating Films on Semiconductors. Proceedings of the International Conference INFOS 85 p.251-4
Editor(s): Simonne, J.J.; Buxo, J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1986 Country of Publication: Netherlands x+265 pp.
ISBN: 0 444 87872 6
Conference Sponsor: CNRS; IEEE; et al
Conference Date: 16-18 April 1985 Conference Location: Toulouse, France

1/3/87
02843132 INSPEC Abstract Number: B87017930
Title: The influence of arsenic S-D implantations on thin oxides
Author(s): Peek, H.L.; Verwey, J.F.
Author Affiliation: Philips Res. Labs., Eindhoven, Netherlands
Conference Title: Insulating Films on Semiconductors. Proceedings of the International Conference INFOS 85 p.199-202
Editor(s): Simonne, J.J.; Buxo, J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1986 Country of Publication: Netherlands x+265 pp.
ISBN: 0 444 87872 6
Conference Sponsor: CNRS; IEEE; et al
Conference Date: 16-18 April 1985 Conference Location: Toulouse, France

1/3/88
02843125 INSPEC Abstract Number: B87017975
Title: Charge injection in thermally grown oxides on silicon-on-sapphire
Author(s): Calligaro, R.B.
Author Affiliation: GEC Res. Labs., Hirst Res. Centre, Wembley, UK
Conference Title: Insulating Films on Semiconductors. Proceedings of the International Conference INFOS 85 p.165-8
Editor(s): Simonne, J.J.; Buxo, J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1986 Country of Publication: Netherlands x+265 pp.
ISBN: 0 444 87872 6
Conference Sponsor: CNRS; IEEE; et al
Conference Date: 16-18 April 1985 Conference Location: Toulouse, France

1/3/89
02843122 INSPEC Abstract Number: B87017974
Title: Endurance of 9.3 nm EEPROM tunnel oxide

Author(s): Faraone, L.
Author Affiliation: RCA Labs., Princeton, NJ, USA
Conference Title: Insulating Films on Semiconductors. Proceedings of the International Conference INFOS 85 p.151-4
Editor(s): Simonne, J.J.; Buxo, J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1986 Country of Publication: Netherlands x+265 pp.
ISBN: 0 444 87872 6
Conference Sponsor: CNRS; IEEE; et al
Conference Date: 16-18 April 1985 Conference Location: Toulouse, France

1/3/90
02843119 INSPEC Abstract Number: B87018175
Title: The switching degradation in floating gate transistors
Author(s): Vollebregt, F.; Verwey, J.F.; Wolters, D.
Author Affiliation: Philips Res. Labs., Eindhoven, Netherlands
Conference Title: Insulating Films on Semiconductors. Proceedings of the International Conference INFOS 85 p.137-40
Editor(s): Simonne, J.J.; Buxo, J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1986 Country of Publication: Netherlands x+265 pp.
ISBN: 0 444 87872 6
Conference Sponsor: CNRS; IEEE; et al
Conference Date: 16-18 April 1985 Conference Location: Toulouse, France

1/3/91
02824186 INSPEC Abstract Number: B87011581
Title: Interaction between deposited film extrinsic gettering and intrinsic gettering in CZ silicon during simulated CMOS process cycles
Author(s): Hahn, S.; Wong, C.-C.D.; Ponce, F.A.; Rek, Z.U.
Author Affiliation: Siltec Corp., Mountain View, CA, USA
Conference Title: Oxygen, Carbon, Hydrogen and Nitrogen in Crystalline Silicon p.353-8
Editor(s): Mikkelsen, J.C., Jr.; Pearton, S.J.; Corbett, J.W.; Pennycook, S.J.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1986 Country of Publication: USA xv+579 pp.
ISBN: 0 931837 24 3
Conference Sponsor: Arco Solar; Cabot Corp.; DOE; Exxon; et al
Conference Date: 2-5 Dec. 1985 Conference Location: Boston, MA, USA

1/3/92
02823551 INSPEC Abstract Number: A87017743, B87011676
Title: Oxide breakdown as a result of charge accumulation during plasma etching
Author(s): Ryden, K.-H.; Norstrom, H.; Nender, C.; Berg, S.
Author Affiliation: Inst. of Microwave Technol., Stockholm, Sweden
Conference Title: 12th Nordic Semiconductor Meeting. Proceedings p. 120-5
Editor(s): Buschmann, F.; Evensen, L.; Hanneborg, A.; Sandmo, H.; Ohlckers, P.
Publisher: Center Ind. Res, Oslo, Norway
Publication Date: 1986 Country of Publication: Norway 386 pp.

ISBN: 82 7267 858 6
Conference Sponsor: R. Norwegian Council Sci. & Ind. Res.; Elektrisk Bur. ; Siemens; Center Ind. Res.; et al
Conference Date: 8-11 June 1986 Conference Location: Jevnaker, Norway

1/3/93
02812330 INSPEC Abstract Number: A87022189
Title: Oxide defect densities and related breakdown lifetimes
Author(s): Chan, C.K.; Waggener, H.A.
Author Affiliation: AT&T Teletype Corp., Skokie, IL, USA
Journal: Thin Solid Films vol.143, no.2 p.119-25
Publication Date: 1 Oct. 1986 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
U.S. Copyright Clearance Center Code: 0040-6090/86/$3.50

1/3/94
02801213 INSPEC Abstract Number: B87006591
Title: Effect of dry etching of a thermal oxide on subsequent growth and properties of thin oxides (approximately=80 AA)
Author(s): Bhattacharyya, A.; Bril, T.; Vorst, C.; Westlund, B.; van Roosmalen, F.
Author Affiliation: Philips Res. Labs., Signetics Corp., Sunnyvale, CA, USA
Journal: Journal of the Electrochemical Society vol.133, no.8 p. 1670-3
Publication Date: Aug. 1986 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

1/3/95
02798239 INSPEC Abstract Number: A87012863, B87006691
Title: Substrate hole current and oxide breakdown
Author(s): Chen, I.C.; Holland, S.; Young, K.K.; Chang, C.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: Applied Physics Letters vol.49, no.11 p.669-71
Publication Date: 15 Sept. 1986 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/86/370669-03$01.00

1/3/96
02789403 INSPEC Abstract Number: B87001758
Title: Input ESD protection networks for fineline NMOS-Effects of stressing waveform and circuit layout
Author(s): DeChiaro, L.F.; Vaidya, S.; Chemeli, R.G.
Author Affiliation: Bell Commun. Res., Murray Hill, NJ, USA
Conference Title: 24th Annual Proceedings Reliability Physics 1986 (Cat. No.86CH2256-6) p.206-14
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA viii+282 pp.
U.S. Copyright Clearance Center Code: CH2256-6/86/0000-0206$01.00
Conference Sponsor: IEEE
Conference Date: 1-3 April 1986 Conference Location: Anaheim, CA, USA

1/3/97
02789398 INSPEC Abstract Number: B87001756
Title: Temperature dependence of CMOS device reliability
Author(s): Yao, C.; Tzou, J.; Cheung, R.; Chan, H.

Author Affiliation: Adv. Micro Devices Inc., Sunnyvale, CA, USA
Conference Title: 24th Annual Proceedings Reliability Physics 1986 (Cat. No.86CH2256-6) p.175-82
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA viii+282 pp.
U.S. Copyright Clearance Center Code: CH2256-6/86/0000-0175$01.00
Conference Sponsor: IEEE
Conference Date: 1-3 April 1986 Conference Location: Anaheim, CA, USA

1/3/98
02789058 INSPEC Abstract Number: B87001753
Title: Measurement of MOS gate-oxide breakdown voltage with protection circuit
Author(s): Araki, Y.
Author Affiliation: Fac. of Eng., Saitama Inst. of Technol., Japan
Journal: Transactions of the Institute of Electronics and Communication Engineers of Japan, Part C vol.J69C, no.6 p.786-8
Publication Date: June 1986 Country of Publication: Japan
CODEN: DTGCAY ISSN: 0373-6113

1/3/99
02785437 INSPEC Abstract Number: A86127193, B87001315
Title: Temperature dependence of charge generation and breakdown in SiO/sub 2/
Author(s): Tzou, J.J.; Yao, C.C.; Cheung, R.; Chan, H.
Author Affiliation: Adv. Micro Devices Inc., Sunnyvale, CA, USA
Journal: IEEE Electron Device Letters vol.EDL-7, no.7 p.446-8
Publication Date: July 1986 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/86/0700-0446$01.00

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02772495 INSPEC Abstract Number: B86067225
Title: Influence of HIC implantations on breakdown properties of thin oxides in planar varactors of dynamic RAMs
Author(s): Schlemm, A.; Mair, T.; Muller, W.; Honlein, W.
Author Affiliation: Siemens AG, Mikroelektronik-Technologiezentrum, Munchen, West Germany
Journal: Siemens Forschungs- und Entwicklungsberichte vol.15, no.4 p.180-6
Publication Date: 1986 Country of Publication: West Germany
CODEN: SFEBBL ISSN: 0370-9736
? t 1/3/101-140

1/3/101
02771927 INSPEC Abstract Number: B86067986
Title: Two-step-temperature oxidation for improved oxide integrity in radiation hardened MOS devices with edge topology
Author(s): Swartz, G.A.
Author Affiliation: RCA Labs., Princeton, NJ, USA
Journal: RCA Review vol.47, no.2 p.154-61
Publication Date: June 1986 Country of Publication: USA
CODEN: RCARCI ISSN: 0033-6831

1/3/102
02770272 INSPEC Abstract Number: A86123430, B86067803
Title: Effect of addition of TCA (trichloroethane) on the electrical

properties of thin oxides processed by a two-step oxidation technique
Author(s): Bhattacharyya, A.; Vorst, C.
Author Affiliation: Philips Res., Labs. Signetics Corp., Sunnyvale, CA, USA
Journal: Journal of Physics D (Applied Physics) vol.19, no.8 p. L161-6
Publication Date: 14 Aug. 1986 Country of Publication: UK
CODEN: JPAPBE ISSN: 0022-3727
U.S. Copyright Clearance Center Code: 0022-3727/86/080161+06$02.50

1/3/103
02741051 INSPEC Abstract Number: B86058544
Title: Improved oxide breakdown by contoured epitaxial island formation
Author(s): Policastro, S.G.; Sullivan, T.E.
Author Affiliation: RCA, Princeton, NJ, USA
Journal: RCA Technical Notes no.1378 p.1-2
Publication Date: 2 July 1986 Country of Publication: USA
CODEN: RCTNAV ISSN: 0483-7495

1/3/104
02713690 INSPEC Abstract Number: B86047486
Title: Thin oxide reliability
Author(s): Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No. 85CH2252-5) p.368-71
Publisher: IEEE, New York, NY, USA
Publication Date: 1985 Country of Publication: USA 772 pp.
U.S. Copyright Clearance Center Code: CH2252-5/85/0000-0368$01.00
Conference Sponsor: IEEE
Conference Date: 1-4 Dec. 1985 Conference Location: Washington, DC, USA

1/3/105
02690741 INSPEC Abstract Number: A86071396, B86041998
Title: Breakdown voltage characteristics of thin oxides and their correlation to defects in the oxide as observed by the EBIC technique
Author(s): Bhattacharyya, A.; Reimer, J.D.; Ritz, K.N.
Author Affiliation: Philips Res. Labs., Sunnyvale, CA, USA
Journal: IEEE Electron Device Letters vol.EDL-7, no.2 p.58-60
Publication Date: Feb. 1986 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/86/0200-0058$01.00

1/3/106
02690377 INSPEC Abstract Number: B86040519
Title: Test system control technique detecting potential short circuit defects by use of a voltage screen
Journal: IBM Technical Disclosure Bulletin vol.28, no.8 p.3582
Publication Date: Jan. 1986 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689

1/3/107
02649718 INSPEC Abstract Number: B86028494
Title: Gate oxide integrity of MOS/SOS devices
Author(s): Swartz, G.A.

Author Affiliation: RCA Labs., Princeton, NJ, USA
Journal: IEEE Transactions on Electron Devices vol.ED-33, no.1 p. 119-25
Publication Date: Jan. 1986 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/86/0100-0119$01.00

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02637060 INSPEC Abstract Number: A86045708
Title: Electron trapping/detrapping in thin SiO/sub 2/ under high fields
Author(s): Wu, N.R.; Chiao, S.; Wang, C.; Bhushan, B.; Yang, C.Y.
Author Affiliation: Gould AMI Semicond., Santa Clara, CA, USA
Conference Title: Thin Films: The Relationship of Structure to Properties p.99-105
Editor(s): Aita, C.R.; SreeHarsha, K.S.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1985 Country of Publication: USA xiii+292 pp.
ISBN: 0 931837 12 X
Conference Sponsor: Mater. Res. Soc
Conference Date: 15-17 April 1985 Conference Location: San Francisco, CA, USA

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02636535 INSPEC Abstract Number: B86021858
Title: The scaling of VLSI; the reliability impact on technology
Author(s): Woods, M.H.
Author Affiliation: Intel Corp., Santa Clara, CA, USA
Conference Title: Proceedings of the Third International Symposium on Very Large Scale Integration Science and Technology. VLSI Science and Technology/1985 p.41-56
Editor(s): Bullis, W.M.; Broydo, S.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1985 Country of Publication: USA viii+564 pp.
Conference Sponsor: Electrochem. Soc
Conference Date: 13-16 May 1985 Conference Location: Toronto, Ont., Canada

1/3/110
02617070 INSPEC Abstract Number: A86028261, B86015294
Title: A quantitative physical model for time-dependent breakdown in SiO/sub 2/
Author(s): Chen, I.C.; Holland, S.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: 23rd Annual Proceedings Reliability Physics 1985 (Cat. No. 85CH2113-9) p.24-31
Publisher: IEEE, New York, NY, USA
Publication Date: 1985 Country of Publication: USA viii+252 pp.
U.S. Copyright Clearance Center Code: CH2113-9/85/0000-0024$01.00
Conference Sponsor: IEEE
Conference Date: 26-28 March 1985 Conference Location: Orlando, FL, USA

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02610730 INSPEC Abstract Number: A86027924, B86014956
Title: Oxide breakdown reliability degradation on Si-gate metal-oxide-semiconductor structure by Al diffusion through polycrystalline

silicon
Author(s): Hokari, Y.
Author Affiliation: VLSI Dev. Div., NEC Corp., Sagamihara, Japan
Journal: Journal of Applied Physics vol.58, no.9 p.3536-40
Publication Date: 1 Nov. 1985 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
U.S. Copyright Clearance Center Code: 0021-8979/85/213536-05$02.40

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02595084 INSPEC Abstract Number: B86009048
Title: Emerging etching techniques
Author(s): Horiike, Y.
Author Affiliation: oshiba Res. & Dev. Center, Kawasaki, Japan
Book Title: VLSI electronics. Microstructure science. Vol.8. Plasma processing for VLSI p.447-86
Editor(s): Einspruch, N.G.; Brown, D.M.
Publisher: Academic Press, London, UK
Publication Date: 1984 Country of Publication: UK xiv+527 pp.
ISBN: 0 12 234108 2

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02571739 INSPEC Abstract Number: A86004170, B86002450
Title: Acceleration factors for thin oxide breakdown
Author(s): McPherson, J.W.; Baglee, D.A.
Author Affiliation: Texas Instrum. Inc., Houston, TX, USA
Journal: Journal of the Electrochemical Society vol.132, no.8 p. 1903-8
Publication Date: Aug. 1985 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

1/3/114
02519461 INSPEC Abstract Number: A85102999, B85050440
Title: A new anisotropic etching of n/sup +/ poly-Si using XeCl excimer laser beam
Author(s): Okano, H.; Sekine, M.; Horiike, Y.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: 1984 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No. 84CH2061-0) p.74-5
Publisher: Japan Soc. Appl. Phys, Tokyo, Japan
Publication Date: 1984 Country of Publication: Japan 94 pp.
ISBN: 4 930813 08 5
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 10-12 Sept. 1984 Conference Location: San Diego, CA, USA

1/3/115
02518789 INSPEC Abstract Number: B85050719
Title: Reliability in MOS integrated circuits
Author(s): Woods, M.H.; Euzent, B.L.
Author Affiliation: Intel Corp., Sanata Clara, CA, USA
Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No. 84CH2099-0) p.50-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1984 Country of Publication: USA 875 pp.
U.S. Copyright Clearance Center Code: CH2099-0/84/0000-0050$01.00
Conference Sponsor: IEEE
Conference Date: 9-12 Dec. 1984 Conference Location: San Francisco,

CA, USA

1/3/116
02495352 INSPEC Abstract Number: B85045809
Title: Ultra sharp trench capacitors formed by peripheral etching
Author(s): Fukano, T.; Ito, T.; Hisatsugu, T.; Ishikawa, H.
Author Affiliation: Fujitsu Labs. Ltd., Atsugi, Japan
Conference Title: Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials p.471-4
Publisher: Business Centre for Acad. Sci. Japan, Tokyo, Japan
Publication Date: 1984 Country of Publication: Japan 2 vol. (ix+721+xix+88) pp.
ISBN: 4 930813 07 7
Conference Sponsor: Japan Soc. Appl. Phys.; IEEE; Electrochem. Soc. Japan ; et al
Conference Date: 30 Aug.-1 Sept. 1984 Conference Location: Kobe, Japan

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02479139 INSPEC Abstract Number: A85076643, B85010625
Title: Characterization of thermally oxidized n/sup +/ polycrystalline silicon
Author(s): Faraone, L.; Vibronek, R.D.; McGinn, J.T.
Author Affiliation: RCA, Princeton, NJ, USA
Journal: IEEE Transactions on Electron Devices vol.ED-32, no.3 p. 577-83
Publication Date: March 1985 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/85/0300-0577$01.00

1/3/118
02469940 INSPEC Abstract Number: A85072134, B85034659
Title: Electrical breakdown in thin gate and tunneling oxides
Author(s): Chen, I.-C.; Holland, S.E.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: IEEE Transactions on Electron Devices vol.ED-32, no.2 p. 413-22
Publication Date: Feb. 1985 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/85/0200-0413$01.00

1/3/119
02409571 INSPEC Abstract Number: B85018457
Title: Oxide thin film for MOS-VLSI circuits
Author(s): Jakubowski, A.; Ruzyllo, J.
Author Affiliation: Inst. Technol. Elektron. Politech., Warszaw, Poland
Journal: Elektronika vol.25, no.7 p.15-19
Publication Date: 1984 Country of Publication: Poland
CODEN: EKNTBZ ISSN: 0033-2089

1/3/120
02409554 INSPEC Abstract Number: B85018440
Title: Reactive ion etching technology for 1 approximately 1.5 mu m VLSI devices
Author(s): Horiike, Y.; Watanabe, T.; Arikado, T.; Hazuki, R.; Sato, M.; Higashikawa, I.; Okano, H.
Author Affiliation: Toshiba Res. & Dev. Center, Kawasaki City, Japan

Conference Title: Proceedings of the International Ion Engineering Congress. The 7th Symposium (1983 International) on Ion Sources and Ion Assisted Technology (ISIAT '83) and the 4th International Conference on Ion and Plasma Assisted Techniques (IPAT '83) p.1579-88 vol.3
Editor(s): Takagi, T.
Publisher: Int. Ion Eng. Congress, Kyoto, Japan
Publication Date: 1983 Country of Publication: Japan 3 vol. 1989 pp.
Conference Sponsor: Inst. Electr. Eng. Japan
Conference Date: 12-16 Sept. 1983 Conference Location: Kyoto, Japan

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02373757 INSPEC Abstract Number: B85006967
Title: Snapback induced gate dielectric breakdown in graded junction MOS structures
Author(s): Shabde, S.N.; Simmons, G.; Baluni, A.; Back, D.
Author Affiliation: Signetics, Sunnyvale, CA, USA
Conference Title: 22nd Annual Proceedings on Reliability Physics 1984 (Catalog No. 84CH1990-1) p.165-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1984 Country of Publication: USA viii+309 pp.
U.S. Copyright Clearance Center Code: CH1990-1/84/0000-0165$01.00
Conference Sponsor: IEEE
Conference Date: 3-5 April 1984 Conference Location: Las Vegas, NV, USA

1/3/122
02372554 INSPEC Abstract Number: B85005643
Title: 22nd Annual Proceedings on Reliability Physics 1984 (Catalog No. 84CH1990-1)
Publisher: IEEE, New York, NY, USA
Publication Date: 1984 Country of Publication: USA viii+309 pp.
Conference Sponsor: IEEE
Conference Date: 3-5 April 1984 Conference Location: Las Vegas, NV, USA

1/3/123
02347544 INSPEC Abstract Number: A84114207, B84059063
Title: On physical models for gate oxide breakdown
Author(s): Holland, S.; Chen, I.C.; Ma, T.P.; Hu, C.
Author Affiliation: Dept. of Electrical Engng. & Computer Sci., Univ. of California, Berkeley, CA, USA
Journal: IEEE Electron Device Letters vol.EDL-5, no.6 p.302-5
Publication Date: Aug. 1984 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/84/0800-0302$01.00

1/3/124
02323080 INSPEC Abstract Number: A84099311, B84052034
Title: Formation of TiSi/sub 2//n/sup +/ poly-Si layer by rapid lamp heating and its application to MOS devices
Author(s): Vachi, T.
Author Affiliation: Musashino Electrical Communication Lab., NTT, Tokyo, Japan
Journal: IEEE Electron Device Letters vol.EDL-5, no.7 p.217-20
Publication Date: July 1984 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106

U.S. Copyright Clearance Center Code: 0741-3106/84/0700-0217$01.00

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02273199 INSPEC Abstract Number: B84036797
Title: Application of high-current ion-implantation systems in semiconductor-device technology
Author(s): Raicu, B.
Author Affiliation: Appl. Implant Technol., Santa Clara, CA, USA
Conference Title: Ion Implantation: Equipment and Techniques. Proceedings of the Fourth International Conference p.450-7
Editor(s): Ryssel, H.; Glawischnig, H.
Publisher: Springer-Verlag, Berlin, West Germany
Publication Date: 1983 Country of Publication: West Germany x+556 pp.
ISBN: 3 540 12491 8
Conference Date: 13-17 Sept. 1982 Conference Location: Berchtesgaden, West Germany

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02273123 INSPEC Abstract Number: B84036721
Title: Reliability problems with VLSI
Author(s): Fantini, F.
Author Affiliation: Reliability & Quality Dept., Telettra, Bologna, Italy
Journal: Microelectronics and Reliability vol.24, no.2 p.275-96
Publication Date: 1984 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
U.S. Copyright Clearance Center Code: 0026-2714/84$3.00+.00

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02256400 INSPEC Abstract Number: A84056853, B84030834
Title: Intrinsic oxide breakdown at near zero electric fields
Author(s): Poorter, T.; Wolters, D.R.
Author Affiliation: Philips Res. Labs., Eindhoven, Netherlands
Conference Title: Insulating Films on Semiconductors. Proceedings of the International Conference INFOS 83 p.266-9
Editor(s): Verweij, J.F.; Wolters, D.R.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1983 Country of Publication: Netherlands xiii+284 pp.
ISBN: 0 444 86735 X
Conference Date: 11-13 April 1983 Conference Location: Eindhoven, Netherlands

1/3/128
02256048 INSPEC Abstract Number: A84056445, B84030463
Title: Electrical properties of thermally-grown SiO/sub 2/ films on N/sup +/ polysilicon
Author(s): Farone, L.
Author Affiliation: RCA Labs., Princeton, NJ, USA
Conference Title: Insulating Films on Semiconductors. Proceedings of the International Conference INFOS 83 p.252-5
Editor(s): Verweij, J.F.; Wolters, D.R.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1983 Country of Publication: Netherlands xiii+284 pp.
ISBN: 0 444 86735 X
Conference Date: 11-13 April 1983 Conference Location: Eindhoven,

Netherlands

1/3/129
02229490 INSPEC Abstract Number: A84046106
Title: Paramagnetic defects in oxidized silicon wafers coated with Langmuir-Blodgett films
Author(s): Roberts, G.G.; Petty, M.C.; Caplan, P.J.; Poindexter, E.H.
Author Affiliation: Dept. of Appl. Phys. & Electronics, Univ. of Durham, Durham, UK
Conference Title: Insulating Films on Semiconductors. Proceedings of the International Conference INFOS 83 p.20-3
Editor(s): Verweij, J.F.; Wolters, D.R.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1983 Country of Publication: Netherlands xiii+284 pp.
ISBN: 0 444 86735 X
Conference Date: 11-13 April 1983 Conference Location: Eindhoven, Netherlands

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02205413 INSPEC Abstract Number: B84014711
Title: Properties of low-pressure CVD tungsten silicide for MOS VLSI interconnections
Author(s): Saraswat, K.C.; Brors, D.L.; Fair, J.A.; Monnig, K.A.; Beyers, R.
Author Affiliation: Integrated Circuits Lab., Stanford Univ., Stanford, CA, USA
Journal: IEEE Transactions on Electron Devices vol.ED-30, no.11 p. 1497-505
Publication Date: Nov. 1983 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/83/1100-1497$01.00

1/3/131
02205260 INSPEC Abstract Number: B84014554
Title: An operational definition for breakdown of thin thermal oxides of silicon
Author(s): Heimann, P.A.
Author Affiliation: Bell Labs., Murray Hill, NJ, USA
Journal: IEEE Transactions on Electron Devices vol.ED-30, no.10 p. 1366-8
Publication Date: Oct. 1983 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/83/1000-1366$01.00

1/3/132
02204430 INSPEC Abstract Number: B84013634
Title: ESD-protected TTL receiver for FET products
Author(s): Chang, H.C.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.26, no.7A p.3122-3
Publication Date: Dec. 1983 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689

1/3/133
02189895 INSPEC Abstract Number: B84009488
Title: Effect of pre-annealing in preventing gate oxide breakdown voltage

degradation induced by polysilicon gate delineation using ion milling
Author(s): Yamauchi, N.; Yachi, T.; Wada, T.
Author Affiliation: Musashino Electrical Communication Lab., Nippon Telegraph & Telephone Public Corp., Tokyo, Japan
Journal: Japanese Journal of Applied Physics, Part 2 (Letters) vol.22, no.8 p.L539-40
Publication Date: Aug. 1983 Country of Publication: Japan
CODEN: JAPLD8 ISSN: 0021-4922

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02175459 INSPEC Abstract Number: B84005399
Title: Model for oxide wearout due to charge trapping (MOS devices)
Author(s): Meyer, W.K.; Crook, D.L.
Author Affiliation: Intel Corp., Aloha, OR, USA
Conference Title: 21st Annual Proceedings on Reliability Physics 1983 p.242-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1983 Country of Publication: USA viii+356 pp.
U.S. Copyright Clearance Center Code: CH1846-5/83/0000-0242$01.00
Conference Sponsor: IEEE
Conference Date: 5-7 April 1983 Conference Location: Phoenix, AZ, USA

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02140609 INSPEC Abstract Number: A83115445
Title: Anodic oxidation of zirconium: Some aspects of the role of foreign ions
Author(s): Panagopoulos, C.
University: Univ. Nottingham, UK
Dissertation Date: 1983
Country of Publication: UK

1/3/136
02128529 INSPEC Abstract Number: A83102817, B83055063
Title: Study of breakdown fields of oxides grown on reactive ion etched silicon surface: improvement of breakdown limits by oxidation of the surface
Author(s): Lifshitz, N.
Author Affiliation: Bell Labs., Murray Hill, NJ, USA
Journal: Journal of the Electrochemical Society vol.130, no.7 p. 1549-50
Publication Date: July 1983 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651

1/3/137
02128413 INSPEC Abstract Number: B83054911
Title: Experimental observation of avalanche multiplication in charge-coupled devices
Author(s): Madan, S.K.; Bhaumik, B.; Vasi, J.M.
Author Affiliation: Centre for Appl. Res. in Electronics, Indian Inst. of Technol., New Delhi, India
Journal: IEEE Transactions on Electron Devices vol.ED-30, no.6 p. 694-9
Publication Date: June 1983 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/83/0600-0694$01.00

1/3/138

02093529 INSPEC Abstract Number: B83043557
Title: Advanced etching process
Author(s): Horiike, Y.; Okano, H.; Shibagaki, M.
Author Affiliation: Toshiba R&D Center, Kanagawa, Japan
Conference Title: Microcircuit Engineering 82. International Conference on Microlithography p.203-10
Publisher: Comite du Colloque International sur la Microlithographie, Grenoble, France
Publication Date: 1982 Country of Publication: France xvi+379 pp.
Conference Sponsor: Ministere de la Recherche et de l'Industrie
Conference Date: 5-8 Oct. 1982 Conference Location: Grenoble, France

1/3/139
02000397 INSPEC Abstract Number: B83012853
Title: Reliability of MOS technologies including MOS power transistors
Author(s): Edwards, D.G.
Author Affiliation: Siemens Corp., Cherry Hill, NJ, USA
Conference Title: Reliability in Electrical and Electronic Components and Systems. Fifth European Conference on Electrotechnics - EUROCON '82 p. 254-8
Editor(s): Lauger, E.; Moltoft, J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1982 Country of Publication: Netherlands xxxvii+1171 pp.
ISBN: 0 444 86419 9
Conference Sponsor: IEEE; Convention Nat. Soc. Electr. Eng. Western Europe
Conference Date: 14-18 June 1982 Conference Location: Copenhagen, Denmark

1/3/140
01962159 INSPEC Abstract Number: A83003345
Title: Electrical conduction and breakdown in oxides of polycrystalline silicon and their correlation with interface texture
Author(s): Heimann, P.A.; Murarka, S.P.; Sheng, T.T.
Author Affiliation: Bell Labs., Murray Hill, NJ, USA
Journal: Journal of Applied Physics vol.53, no.9 p.6240-5
Publication Date: Sept. 1982 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
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$98.00 140 Type(s) in Format 3
$0.00 15 Type(s) in Format 6 (UDF)
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$1.50 Dialnet
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MAILED TO: RL/ERDR (D. Burns)
Griffiss AFB NY 13441-5700

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Approving Authority

Name/Title of Air Force
Approving Authority

Organization/Location

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